

|              |          |   |
|--------------|----------|---|
| <b>SANYO</b> | No.4363B | <b>LC6527N/F/L, 6528N/F/L</b>   |
|              |          | SINGLE-CHIP 4-BIT MICROCOMPUTER FOR<br>SMALL-SCALE CONTROL-ORIENTED<br>APPLICATIONS |

## Overview

The LC6527N/F/L, LC6528N/F/L belong to our single-chip 4-bit microcomputer LC6500 series fabricated using CMOS process technology and are suited for use in small-scale control-oriented applications. Their basic architecture and instruction set are the same. Application areas include the standard logic circuits and applications where the number of controls is small. The LC6527N/F/L, LC6528N/F/L have relation to the LC6527C/H, LC6528C/H. The C version can be replaced by N version, and the H version by F version (a part of the function is different). The L version is added as a low voltage version. The following show the careful difference of C and N version when you replace C version with N version.

|                         |               | C version           | N version              |
|-------------------------|---------------|---------------------|------------------------|
| Operating Temperature   |               | -30°C to +70°C      | -40°C to +85°C         |
| 1-pin C oscillation     |               | exist               | not exist              |
| CF Oscillation Constant | 400kHz MURATA | C1=C2=330pF<br>R=0Ω | C1=C2=220pF<br>R=2.2kΩ |
|                         | 800kHz MURATA | C1=C2=220pF<br>R=0Ω | C1=C2=100pF<br>R=2.2KΩ |
|                         |               | C1=C2=220pF<br>R=0Ω | C1=C2=100pF<br>R=0Ω    |
|                         | 1MHz MURATA   | C1=C2=220pF<br>R=0Ω | C1=C2=100PF<br>R=2.2kΩ |

\* 2-pin CR fixed-frequency oscillator with small frequency tolerance.

\*\* Other options shown in table on the left.

(Note) The suffix of recommend oscillation is changed C version and N version, but the characteristics are no change.

## Features

- 1) CMOS technology for a low-power operation (with instruction-controlled standby function)
- 2) ROM/RAM  
LC6527N/F/L ROM : 1K x 8bits, RAM : 64 x 4bits  
LC6528N/F/L ROM : 0.5K x 8bits, RAM : 32 x 4bits
- 3) Instruction set : 51 kinds selectable from 80 instructions common to the LC6500 series
- 4) Wide operating voltage range form 2.2V to 6.0V (L version)
- 5) Instruction cycle time of 0.92μs (F version)

Continued on next page.

Continued from preceding page.

## 6) Flexible I/O port

- Number of ports : 4 ports/13 pins max.
- All ports : Input/output common  
Input/output voltage 15V max. (open drain type)  
Output current 20mA max. (sink current) (LED direct drivable)
- Option selectable for your intended system
  - A. Open drain output, pull-up resistor : Single-bit select for all ports
  - B. Output level at the reset mode : 4-bit select of H/L level for port C/D

## 7) Stack level : 4 levels

## 8) Timer : 4-bit prescaler + 8-bit programmable timer

## 9) Clock oscillation option selectable for your intended system

- Oscillator option : 2-pin RC oscillation (N, L version)  
2-pin ceramic resonator oscillation, 1-pin external clock input (N,F,L version)
- Predivider option : No predivider, 1/3 predivider, 1/4 predivider (N, L version)

Function Table

| Item              |                            | LC6527N/28N   | LC6527F/28F                               | LC6527L/28L   |
|-------------------|----------------------------|---|---|---|
| Memory            | ROM                        | 1024 x 8 bits (27N)<br>512 x 8 bits (28N)   | 1024 x 8 bits (27F)<br>512 x 8 bits (28F) | 1024 x 8 bits (27L)<br>512 x 8 bits (28L)               |
|                   | RAM                        | 64 x 4 bits (27N)<br>32 x 4 bits (28N)  | 64 x 4 bits (27F)<br>32 x 4 bits (28F)    | 64 x 4 bits (27L)<br>32 x 4 bits (28L)                  |
| Instruction       | Instruction set            | 51  | 51  | 51  |
| On-chip function  | Timer                      | 4-bit prescaler + 8-bit timer   | 4-bit prescaler + 8-bit timer             | 4-bit prescaler + 8-bit timer                           |
|                   | Stack level                | 4   | 4   | 4   |
|                   | Standby function           | Standby available<br>by HALT instruction  | Standby available<br>by HALT instruction  | Standby available<br>by HALT instruction                |
| Input/output port | Number of ports            | I/O 13 max.   | I/O 13 max.                               | I/O 13 max.   |
|                   | I/O voltage                | 15V max.  | 15V max.                                  | 15V max.  |
|                   | Output current             | 10mA typ. 20mA max.   | 10mA typ. 20mA max.                       | 10mA typ. 20mA max.                                     |
|                   | I/O circuit configuration  | Open drain (N channel) or pull-up resistor-provided output selectable bit by bit. |   |   |
|                   | Output level at reset mode | "H" or "L" level selectable port by port (port C, D only)                         |   |   |
| Characteristic    | Minimum cycle time         | 2.77μs (VDD≥4V)<br>6.0μs (VDD≥3V)   | 0.92μs (VDD≥4.5V)                         | 3.84μs (VDD≥2.2V)                                       |
|                   | Supply voltage             | 3 to 6V   | 4.5 to 6V                                 | 2.2 to 6V   |
|                   | Current dissipation        | 2.5mA typ.  | 4mA typ.                                  | 2.5mA typ.  |
| Oscillation       | Resonator                  | RC (850kHz, 400kHz typ.)<br>ceramic (400k, 800k, 1MHz,<br>4MHz)                   | ceramic 4MHz                              | RC (400kHz typ.)<br>ceramic (400k, 800k, 1MHz,<br>4MHz) |
|                   | predivider option          | 1/1, 1/3, 1/4   | 1/1                                       | 1/1, 1/3, 1/4   |
| Other             | Package                    | DIP18, MFP18*   | DIP18, MFP18*                             | DIP18, MFP18*   |

(Note) Information on the resonator and oscillation circuit constants will be presented as soon as the recommended circuit is determined.

\* MFP18 : under development

# Pin Assignment

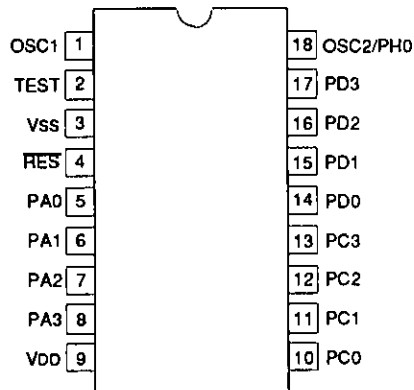
LC6527N/F/L

LC6528N/F/L

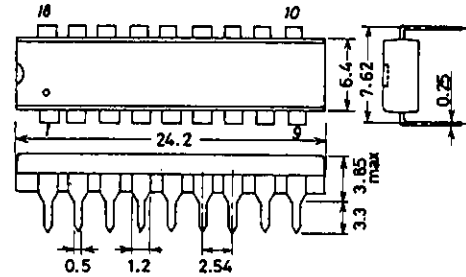
# Package Dimensions

3007A

(unit : mm)



Common to DIP • MFP

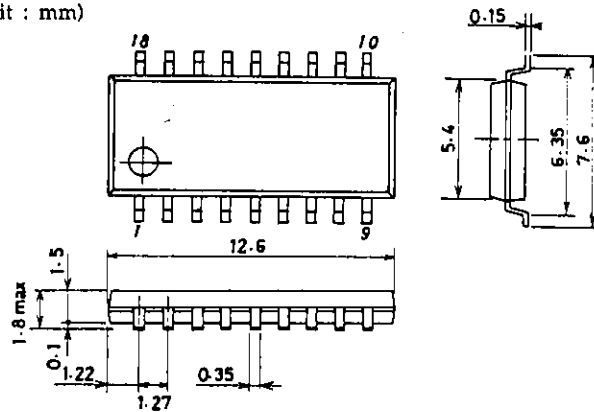


SANYO : DIP18

3095-M181C

(unit : mm)

Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.



SANYO : MFP18

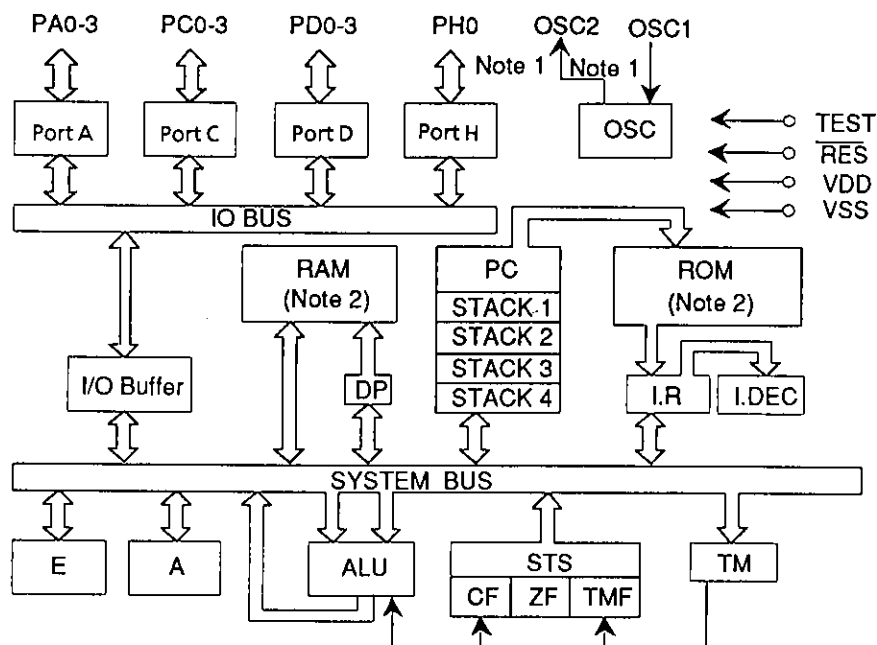
(Note) The package is the reference figure without the description of the rank. Please inquire us for the formal package.

# Pin Name

|            |                                     |      |                                |
|------------|-------------------------------------|------|--------------------------------|
| OSC1, OSC2 | : C, R or ceramic resonator for OSC | PH 0 | : Input/output common port H 0 |
| RES        | : Reset                             | TEST | : Test                         |
| PA 0-3     | : Input/output common port A 0-3    |      |                                |
| PC 0-3     | : Input/output common port C 0-3    |      |                                |
| PD 0-3     | : Input/output common port D 0-3    |      |                                |

## System Block Diagram

LC6527N/F/L, LC6528N/F/L



Note 1. The PH0 pin or OSC2 pin is selected by the mask option.

Note 2. LC6527N/F/L ROM : 1024 bytes RAM : 64 words  
 LC6528N/F/L ROM : 512 bytes RAM : 32 words

## Development Support Tools

The following are available to support the program development for the LC6527, LC6528.

### (1) User's Manual

"LC6527, LC6528 User's Manual" No. 24-6016 ('86.10.1.)

Note : Do not use "LC6523 Series User's Manual" No. 16A-7015 and No. 16-9064.

### (2) Development Tool Manual

For the EVA-800 or the EVA-850 system, refer to "EVA-800. LC6527, LC6528 Development Tool Manual".

### (3) Development Tools

#### A. For program evaluation

1. Piggy back (LC65PG23/26)

2. 23T27 ; The pin-to-pin conversion socket for the piggy back LC65PG23/26.

#### B. For program evaluation

29 TO 27 ; The pin-to-pin conversion socket for EPROM built-in microcomputer (LC65E29)

Note. For notes for program evaluation, do not fail to refer to '4-3. Notes when evaluating programs' in "LC6527, LC6528 User's Manual".

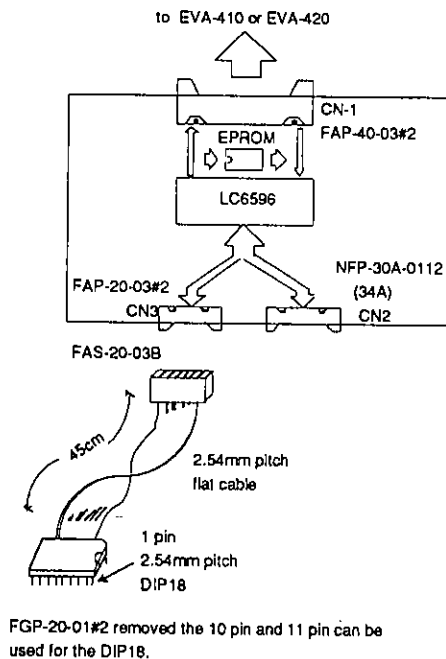


Fig. 1 Evaluation kit target board  
(EVA-TB6523C/26C/27C/28C)

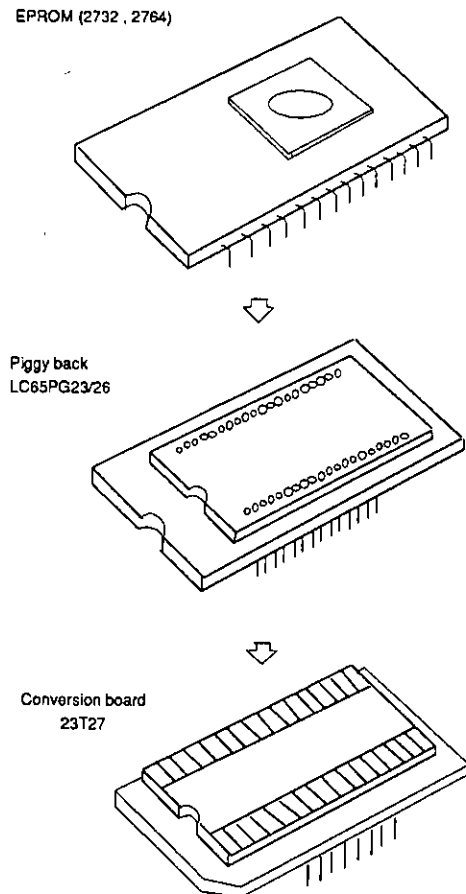


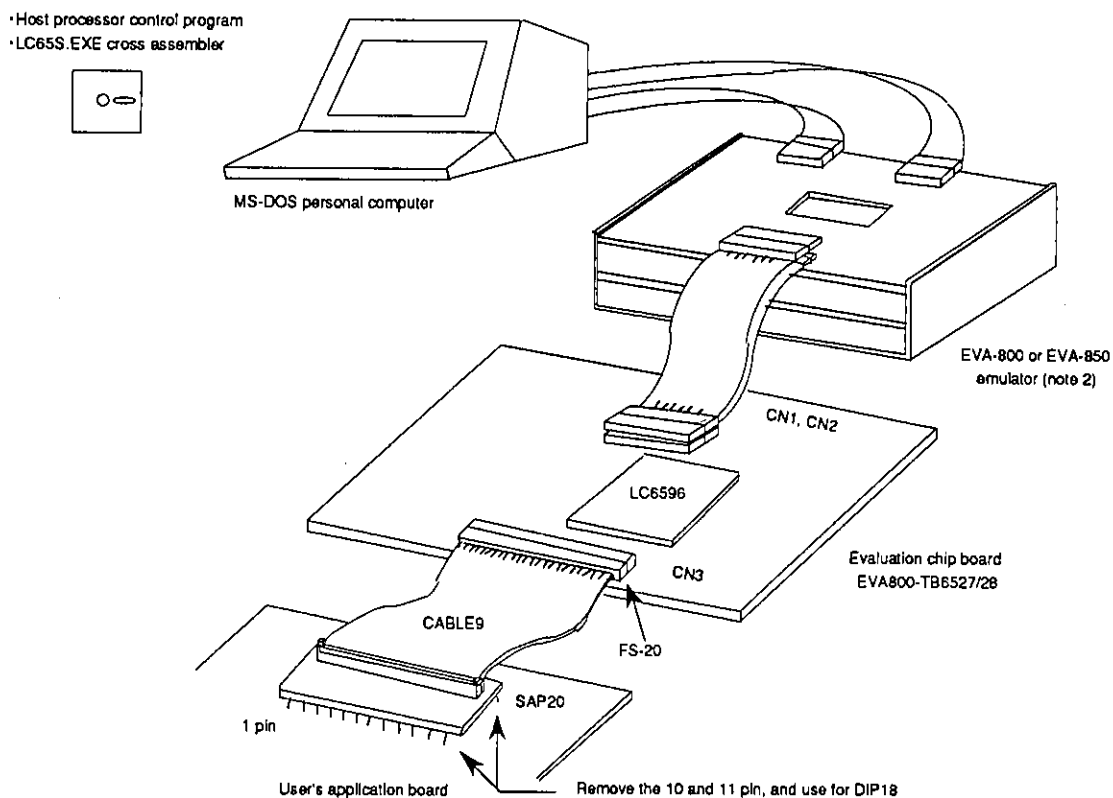
Fig. 2 Program evaluation

C. For program development (EVA-800 or EVA-850 system) —

1. MS-DOS for host system (Note 1)
2. Cross assembler.....MS-DOS base cross assembler : <LC65S.EXE>
3. Host control program
4. Evaluation chip : LC6596
5. Emulator : EVA-800 or EVA-850 emulator and evaluation boards EVA800-TB6527/28

D. For program development (EVA-86000 system) under development

Appearance of Development Support System



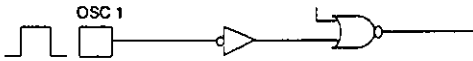
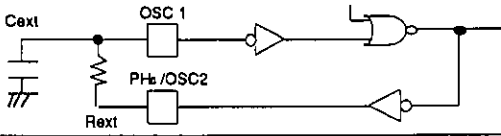
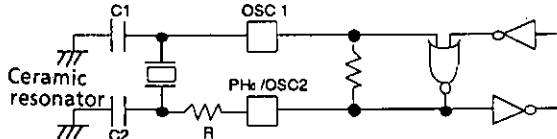
(Note 1) MS-DOS : Trademark of Microsoft Corporation

(Note 2) The EVA-800, EVA-850 are general term for emulator. A suffix (A, B,...) is added at the end of EVA-800 and EVA-850 as they are improved to be a newer version. Do not use the EVA-800 and EVA-850 with no suffix added.

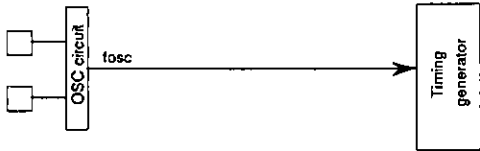
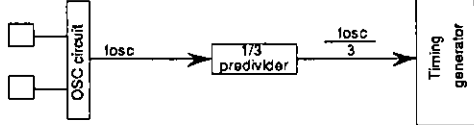
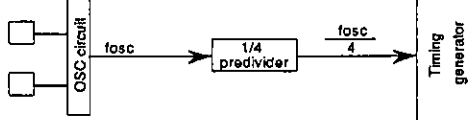
## Pin Description

| Pin Name     | Pins | I/O          | Function  | Option  | Reset Mode  |
|--------------|------|--------------|---|---|---|
| VDD          | 1    | —            | Power supply  | —   | —   |
| VSS          | 1    | —            |   |   |   |
| OSC1         | 1    | Input        | <ul style="list-style-type: none"> <li>Pin for externally connecting RC, ceramic resonator for system clock generation.</li> <li>For 1-pin external clock input, the PH0/OSC2 pin is used as I/O port PH0.</li> <li>For 2-pin RC OSC, 2-pin ceramic resonator OSC, the PH0/OSC2 pin is used as OSC pin OSC2.</li> </ul>   | 1) 1-pin external clock input<br>2) 2-pin RC OSC<br>3) 2-pin ceramic resonator OSC<br>4) Predivider option<br>1. No predivider<br>2. 1/3 predivider<br>3. 1/4 predivider                            | —   |
| PA 0 to PA 3 | 4    | Input/output | <ul style="list-style-type: none"> <li>I/O port A0 to 3</li> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instruction)</li> <li>Single-bit set/reset (SPB, RPB instruction)</li> <li>Standby is controlled by PA3.</li> <li>The PA3 pin must be free from chattering during the HALT instruction execution cycle.</li> </ul> | 1) Open drain type output<br>2) With pull-up resistor<br>1), 2) : Specified bit by bit  | • "H" output (Output Nch transistor : OFF)            |
| PC 0 to PC 3 | 4    | Input/output | <ul style="list-style-type: none"> <li>I/O port C0 to 3</li> <li>Same as for PA0 to 3 (Note)</li> <li>Option permits output at the reset mode to be "H" or "L".</li> <li>(Note) No standby control function is provided.</li> </ul>   | 1) Open drain type output<br>2) With pull-up resistor<br>3) Output at reset mode: "H"<br>4) Output at reset mode: "L"<br>• 1), 2): Specified bit by bit<br>• 3), 4): Specified in a group of 4 bits | • "H" output<br>• "L" output<br>(Option - selectable) |
| PD 0 to PD 3 | 4    | Input/output | <ul style="list-style-type: none"> <li>I/O port D0 to 3</li> <li>Same as for PC0 to 3</li> </ul>  | Same as for PC0 to 3  | Same as for PC0 to 3                                  |
| PH 0 / OSC2  | 1    | Input/output | <ul style="list-style-type: none"> <li>I/O port H0</li> <li>Same as for PA0 to 3 (Note)</li> <li>Single-bit configuration</li> <li>For 2-pin OSC, this pin is used as the OSC2 pin, providing no function as I/O port.</li> <li>(Note) No standby control function is provided.</li> </ul>  | Same as for PA0 to 3  | Same as for PA0 to 3                                  |
| RES          | 1    | Input        | <ul style="list-style-type: none"> <li>System reset input</li> <li>For power-up reset, C is connected externally.</li> <li>For reset restart, "L" level is applied for 4 clock cycles or more.</li> </ul>   |   |   |
| TEST         | 1    | Input        | <ul style="list-style-type: none"> <li>LSI test pin</li> <li>Normally connected to VSS</li> </ul>   |   |   |

### Oscillator circuit option

| Option Name              | Circuit   | Conditions, etc.  |
|--------------------------|---|---|
| 1. External clock        |  | The PH 0 / OSC2 pin is used as port PH0.                                    |
| 2. 2-pin RC OSC          |  | The PH 0 / OSC2 pin is used as OSC pin OSC2, providing no function as port. |
| 3. Ceramic resonator OSC |  | The PH 0 / OSC2 pin is used as OSC pin OSC2, providing no function as port. |

### Predivider Option

| Option Name            | Circuit   | Conditions, etc.   |
|------------------------|---|--|
| 1. No predivider (1/1) |   | <ul style="list-style-type: none"> <li>• Applicable to all of 3 OSC options.</li> <li>• The OSC frequency, external clock do not exceed 1444kHz. (LC6527N, 6528N)</li> <li>• The OSC frequency, external clock do not exceed 4330kHz. (LC6527F, 6528F)</li> <li>• The OSC frequency, external clock do not exceed 1040kHz. (LC6527L, 6528L)</li> </ul> |
| 2. 1/3 predivider      |  | <ul style="list-style-type: none"> <li>• Applicable to only 2 OSC options of external clock, ceramic resonator OSC.</li> <li>• The OSC frequency, external clock do not exceed 4330kHz.</li> </ul>   |
| 3. 1/4 predivider      |  | <ul style="list-style-type: none"> <li>• Applicable to only 2 OSC options of external clock, ceramic resonator OSC.</li> <li>• The OSC frequency, external clock do not exceed 4330kHz.</li> </ul>   |

Note : The OSC option and predivider option are summarized below. Full care must be exercised.



Table of OSC, predivider-Option of LC6527N/28N, 27F/28F and 27L/28L

## LC6527N, L6528N

| Circuit Configuration                                   | Frequency   | Predivider Option<br>(Cycle Time) | VDD Range | Remarks                           |
|---|---|-----------------------------------|-----------|-----------------------------------|
| Ceramic resonator OSC                                   | 400kHz  | 1/1 (10 μs)                       | 3 to 6V   | Unusable with 1/3, 1/4 predivider |
|   | 800kHz  | 1/1 (5 μs)                        | 4 to 6V   |                                   |
|   |   | 1/3 (15 μs)                       | 4 to 6V   |                                   |
|   |   | 1/4 (20 μs)                       | 4 to 6V   |                                   |
|   | 1MHz  | 1/1 (4 μs)                        | 4 to 6V   |                                   |
|   |   | 1/3 (12 μs)                       | 4 to 6V   |                                   |
|   |   | 1/4 (16 μs)                       | 4 to 6V   |                                   |
|   | 4MHz  | 1/3 (3 μs)                        | 4 to 6V   | Unusable with 1/1 predivider      |
| 1/4 (4 μs)  |   | 4 to 6V                           |           |                                   |
| 1-pin external clock                                    | 200k to 667kHz  | 1/1 (20 to 6μs)                   | 3 to 6V   |                                   |
|   | 600k to 2000kHz   | 1/3 (20 to 6μs)                   | 3 to 6V   |                                   |
|   | 800k to 2667kHz   | 1/4 (20 to 6μs)                   | 3 to 6V   |                                   |
|   | 200k to 1444kHz   | 1/1 (20 to 2.77μs)                | 4 to 6V   |                                   |
|   | 600k to 4330kHz   | 1/3 (20 to 2.77μs)                | 4 to 6V   |                                   |
|   | 800k to 4330kHz   | 1/4 (20 to 3.70μs)                | 4 to 6V   |                                   |
| External clock by 2-pin RC OSC circuit                  | Same as above   |                                   |           |                                   |
| 2-pin RC  | Used with 1/1predivider,recommended constants. If used with other than recommended constants, the frequency, predivider option, VDD range must be the same as for 1-pin external clock. |                                   | 3 to 6V   |                                   |
|   |   |                                   | 4 to 6V   |                                   |
| External clock input to the ceramic oscillation circuit | The ceramic oscillation circuit cannot be driven by external clock.<br>To drive the circuit with external clock, select the external clock option or the 2-pin RC option.               |                                   |           |                                   |

## LC6527F, L6528F

| Circuit Configuration                                   | Frequency  | Predivider Option<br>(Cycle Time) | VDD Range | Remarks |
|---|--|-----------------------------------|-----------|---------|
| Ceramic resonator OSC                                   | 4MHz   | 1/1 (1 $\mu$ s)                   | 4.5 to 6V |         |
| 1-pin external clock                                    | 200k to 4330kHz  | 1/1 (20 to 0.92 $\mu$ s)          | 4.5 to 6V |         |
| External clock input to the ceramic oscillation circuit | The ceramic oscillation circuit cannot be driven by external clock.<br>To drive the circuit with external clock, select the external clock option. |                                   |           |         |

## LC6527L, L6528L

| Circuit Configuration                                   | Frequency   | Predivider Option (Cycle Time) | VDD Range | Remarks                           |
|---|---|--------------------------------|-----------|-----------------------------------|
| Ceramic resonator OSC                                   | 400kHz  | 1/1 (10 $\mu$ s)               | 2.2 to 6V | Unusable with 1/3, 1/4 predivider |
|   | 800kHz  | 1/1 (5 $\mu$ s)                | 2.2 to 6V |                                   |
|   |   | 1/3 (15 $\mu$ s)               | 2.2 to 6V |                                   |
|   |   | 1/4 (20 $\mu$ s)               | 2.2 to 6V |                                   |
|   | 1MHz  | 1/1 (4 $\mu$ s)                | 2.2 to 6V |                                   |
|   |   | 1/3 (12 $\mu$ s)               | 2.2 to 6V |                                   |
|   |   | 1/4 (16 $\mu$ s)               | 2.2 to 6V |                                   |
|   | 4MHz  | 1/4 (4 $\mu$ s)                | 2.2 to 6V | Unusable with 1/1, 1/3 predivider |
| 1-pin external clock                                    | 200k to 1040kHz   | 1/1 (20 to 3.84 $\mu$ s)       | 2.2 to 6V |                                   |
|   | 600k to 3120kHz   | 1/3 (20 to 3.84 $\mu$ s)       | 2.2 to 6V |                                   |
|   | 800k to 4160kHz   | 1/4 (20 to 3.84 $\mu$ s)       | 2.2 to 6V |                                   |
| External clock by 2-pin RC OSC circuit                  | Same as above   |                                |           |                                   |
| 2-pin RC  | Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the frequency, predivider option, VDD range must be the same as for 1-pin external clock. |                                | 2.2 to 6V |                                   |
| External clock input to the ceramic oscillation circuit | The ceramic oscillation circuit cannot be driven by external clock.<br>To drive the circuit with external clock, select the external clock option or the 2-pin RC option.                 |                                |           |                                   |

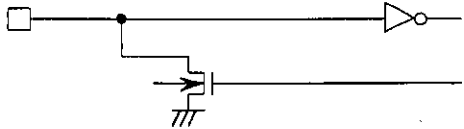
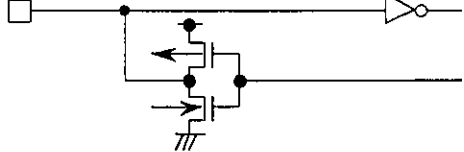
## Option of ports C, D Output Level at the Reset Mode

For input/output common ports C, D either of the following two output levels may be selected in a group of 4 bits during reset by option.

| Option Name                             | Conditions , etc.           |
|---|-----------------------------|
| 1. Output at the reset mode : "H" level | All of 4 bits of ports C, D |
| 2. Output at the reset mode : "L" level | All of 4 bits of ports C, D |

## Option of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option.

| Option Name                     | Circuit   | Conditions , etc.   |
|---------------------------------|---|---|
| 1. Open drain output            |  | <ul style="list-style-type: none"> <li>Unapplicable to port PH0/OSC2 when 2-pin RC OSC or ceramic resonator OSC is selected.</li> </ul> |
| 2. Output with pull-up resistor |  |   |

**LC6527N, 6528N****1. Absolute Maximum Ratings at Ta=25°C, VSS=0V**

| Parameter                   | Symbol          | Conditions                                    | Pins                  | Limits                            | unit |
|-----------------------------|-----------------|---|-----------------------|-----------------------------------|------|
| Maximum supply voltage      | VDD max         |   | VDD                   | -0.3 to +7.0                      | V    |
| Output voltage              | VO              |   | OSC2                  | Allowable up to voltage generated | V    |
| Input voltage               | VI(1)           |   | OSC1 (*1)             | -0.3 to VDD+0.3                   | V    |
|                             | VI(2)           |   | TEST, RES             | -0.3 to VDD+0.3                   | V    |
| Input/output voltage        | VIO(1)          |   | Port of OD type       | -0.3 to +15                       | V    |
|                             | VIO(2)          |   | Port of PU type       | -0.3 to VDD+0.3                   | V    |
| Peak output current         | IOP             |   | I/O port              | -2 to +20                         | mA   |
| Average output current      | IOA             | Per pin over the period of 100 ms             | I/O Port              | -2 to +20                         | mA   |
|                             | $\Sigma$ IOA(1) | Total current of PA0 to 3, (*2)               | PA0 to 3              | -6 to +40                         | mA   |
|                             | $\Sigma$ IOA(2) | Total current of PC0 to 3, PD0 to 3, PH0 (*2) | PC0 to 3 PH0 PD0 to 3 | -14 to +90                        | mA   |
| Allowable power dissipation | Pd max(1)       | Ta=-40 to +85°C (DIP package)                 |                       | 250                               | mW   |
|                             | Pd max(2)       | Ta=-40 to +85°C (MFP package)*                |                       | 150                               | mW   |
| Operating temperature       | Topr            |   |                       | -40 to +85                        | °C   |
| Storage temperature         | Tstg            |   |                       | -55 to +125                       | °C   |

\* ..... Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

**2. Allowable Operating Conditions at Ta=-40 to +85°C, VSS=0V, VDD=3.0 to 6.0V**

| Parameter                | Symbol | Conditions              | VDD [V]    | Pins                        | Limits |      |         |      |
|--------------------------|--------|-------------------------|------------|-----------------------------|--------|------|---------|------|
|                          |        |                         |            |                             | min.   | typ. | max.    | unit |
| Operating supply voltage | VDD    |                         |            | VDD                         | 3.0    |      | 6.0     | V    |
| Standby supply voltage   | VST    | RAM, register hold (*3) |            | VDD                         | 1.8    |      | 6.0     | V    |
| "H"-level input voltage  | VIH(1) | Output Nch Tr. OFF      |            | Port of OD type (except H0) | 0.7VDD |      | +13.5   | V    |
|                          | VIH(2) | Output Nch Tr. OFF      |            | Port of PU type (except H0) | 0.7VDD |      | VDD     | V    |
|                          | VIH(3) | Output Nch Tr. OFF      |            | H0 of OD type               | 0.8VDD |      | +13.5   | V    |
|                          | VIH(4) | Output Nch Tr. OFF      |            | H0 of PU type               | 0.8VDD |      | VDD     | V    |
|                          | VIH(5) |                         |            | RES                         | 0.8VDD |      | VDD     | V    |
|                          | VIH(6) | External clock mode     |            | OSC1                        | 0.8VDD |      | VDD     | V    |
| "L"-level input voltage  | VIL(1) | Output Nch Tr. OFF      | VDD=4 to 6 | Port                        | VSS    |      | 0.3VDD  | V    |
|                          | VIL(2) | Output Nch Tr. OFF      | VDD=3 to 6 | Port                        | VSS    |      | 0.25VDD | V    |
|                          | VIL(3) | External clock mode     | VDD=4 to 6 | OSC1                        | VSS    |      | 0.25VDD | V    |

| Parameter                           | Symbol       | Conditions  | Pins                                  | Limits                     |            |                                |  |
|-------------------------------------|--------------|---|---------------------------------------|----------------------------|------------|--------------------------------|--|
|                                     |              |   |                                       | min.                       | typ.       | max.                           | unit                                   |
| "L"-level input voltage             | VIL(4)       | External clock mode   | VDD=3 to 6<br>OSC1                    | VSS                        |            | 0.2VDD                         | V                                      |
|                                     | VIL(5)       |   | VDD=4 to 6<br>TEST                    | VSS                        |            | 0.3VDD                         | V                                      |
|                                     | VIL(6)       |   | VDD=3 to 6<br>TEST                    | VSS                        |            | 0.25VDD                        | V                                      |
|                                     | VIL(7)       |   | VDD=4 to 6<br>$\overline{\text{RES}}$ | VSS                        |            | 0.25VDD                        | V                                      |
|                                     | VIL(8)       |   | VDD=3 to 6<br>$\overline{\text{RES}}$ | VSS                        |            | 0.2VDD                         | V                                      |
| Operating frequency (cycle time)    | fop (Tcyc)   | When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.33MHz. | VDD=4 to 6                            | 200<br>(20)<br>200<br>(20) |            | 1444<br>(2.77)<br>667<br>(6.0) | kHz<br>( $\mu$ s)<br>kHz<br>( $\mu$ s) |
| External clock conditions           |              |   |                                       |                            |            |                                |  |
| Frequency                           | text         | Fig.1.<br>When clock exceeds 1.444  | VDD=4 to 6<br>3 to 6                  | OSC1                       | 200<br>200 | 4330<br>2667                   | kHz<br>kHz                             |
| Pulse width                         | textH, textL | MHz, the 1/3 or 1/4 pre-  | VDD=4 to 6<br>3 to 6                  | OSC1                       | 69<br>180  |                                | ns<br>ns                               |
| Rise/Fall time                      | textR, textF | divider option is selected.   | VDD=4 to 6<br>3 to 6                  | OSC1                       |            | 50<br>100                      | ns<br>ns                               |
| Oscillation guar-<br>anty constants |              |   |                                       |                            |            |                                |  |
| 2-pin RC<br>oscillation             | Cext         | Fig.2   | VDD=3 to 6                            | OSC1, OSC2                 |            | 220 $\pm$ 5%                   | pF                                     |
|                                     | Cext         | Fig.2   | VDD=4 to 6                            | OSC1, OSC2                 |            | 220 $\pm$ 5%                   | pF                                     |
|                                     | Rext         | Fig.2   | VDD=3 to 6                            | OSC1, OSC2                 |            | 12 $\pm$ 1%                    | k $\Omega$                             |
|                                     | Rext         | Fig.2   | VDD=4 to 6                            | OSC1, OSC2                 |            | 4.7 $\pm$ 1%                   | k $\Omega$                             |
| Ceramic resonator OSC               |              | Fig.3   |                                       |                            |            | Table 1                        |  |

## 3. Electrical Characteristics at Ta=-40 to +85°C, VSS=0V, VDD=3.0V to 6.0V

| Parameter                | Symbol | Conditions   | Pins                    | Limits  |       |      |         |
|--------------------------|--------|--|-------------------------|---------|-------|------|---------|
|                          |        |  |                         | min.    | typ.  | max. | unit    |
| "H"-level input current  | IIH(1) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.)<br>VIN=+13.5V | Port of OD type         |         |       | +5.0 | $\mu$ A |
|                          | IIH(2) | External clock mode,<br>VIN=VDD  | OSC1                    |         |       | +1.0 | $\mu$ A |
| "L"-level input current  | IIL(1) | Output Nch Tr. OFF<br>VIN=VSS  | Port of OD type         | -1.0    |       |      | $\mu$ A |
|                          | IIL(2) | Output Nch Tr. OFF<br>VIN=VSS  | Port of PU type         | -1.3    | -0.35 |      | mA      |
|                          | IIL(3) | VIN=VSS  | $\overline{\text{RES}}$ | -45     | -10   |      | $\mu$ A |
|                          | IIL(4) | External clock mode,<br>VIN=VSS  | OSC1                    | -1.0    |       |      | $\mu$ A |
| "H"-level output voltage | VOH(1) | IOH=-50 $\mu$ A<br>VDD=4.0 to 6.0V                                       | Port of PU type         | VDD-1.2 |       |      | V       |
|                          | VOH(2) | IOH=-10 $\mu$ A  | Port of PU type         | VDD-0.5 |       |      | V       |

| Parameter   | Symbol      | Conditions  | Pins   | Limits                    |                            |                            |                          |
|---|-------------|---|--|---------------------------|----------------------------|----------------------------|--------------------------|
|   |             |   |  | min.                      | typ.                       | max.                       | unit                     |
| "L"-level output voltage                          | VOL(1)      | IOL=10mA, VDD=4.0 to 6.0V   | Port   |                           |                            | 1.5                        | V                        |
|   | VOL(2)      | IOL=1.8mA, IOL of each port: 1mA or less  | Port   |                           |                            | 0.4                        | V                        |
| Hysteresis voltage                                | VHIS        |   | $\overline{\text{RES}}$ , OSC1 of schmitt type(*4)   |                           | 0.1VDD                     |                            | V                        |
| Current dissipation 2-pin RC oscillation          | IDDOP(1)    | Output Nch Tr. OFF at operating, Port=VDD<br>Fig.2 fosc=850kHz (TYP)<br>VDD=4 to 6V   | VDD  |                           | 1.0                        | 2.5                        | mA                       |
| Ceramic resonator oscillation                     | IDDOP(2)    | Fig.2 fosc=400kHz (TYP)   | VDD  |                           | 0.8                        | 2.5                        | mA                       |
|   | IDDOP(3)    | Fig.3 4MHz, 1/3 predivider<br>VDD=4 to 6V   | VDD  |                           | 1.2                        | 3                          | mA                       |
|   | IDDOP(4)    | Fig.3 4MHz, 1/4 predivider<br>VDD=4 to 6V   | VDD  |                           | 1.2                        | 2.5                        | mA                       |
|   | IDDOP(5)    | Fig.3 400kHz  | VDD  |                           | 0.5                        | 2                          | mA                       |
| External clock                                    | IDDOP(6)    | Fig.3 800kHz VDD=4 to 6V  | VDD  |                           | 1.0                        | 2.5                        | mA                       |
|   | IDDOP(7)    | 200kHz to 667kHz,<br>1/1 predivider<br>600kHz to 2000kHz,<br>1/3 predivider<br>800kHz to 2667kHz,<br>1/4 predivider                         | VDD  |                           | 1.0                        | 2.5                        | mA                       |
|   | IDDOP(8)    | 200kHz to 1444kHz,<br>1/1 predivider<br>600kHz to 4330kHz,<br>1/3 predivider<br>800kHz to 4330kHz,<br>1/4 predivider, VDD=4 to 6V           | VDD  |                           | 1.2                        | 3                          | mA                       |
| Standby mode                                      | IDDst       | Output Nch Tr.OFF VDD=6V  | VDD  |                           | 0.05                       | 10                         | $\mu\text{A}$            |
|   |             | Port=VDD VDD=3V   | VDD  |                           | 0.025                      | 5                          | $\mu\text{A}$            |
| Oscillation characteristics Ceramic OSC Frequency | fCFOSC (*5) | Fig.3 fo=400kHz<br>Fig.3 fo=800kHz, VDD=4 to 6V<br>Fig.3 fo=1MHz VDD=4 to 6V<br>Fig.3 fo=4MHz, 1/3 predivider<br>1/4 predivider VDD=4 to 6V | OSC1, OSC2<br>OSC1, OSC2<br>OSC1, OSC2<br>OSC1, OSC2 | 384<br>768<br>960<br>3840 | 400<br>800<br>1000<br>4000 | 416<br>832<br>1040<br>4160 | kHz<br>kHz<br>kHz<br>kHz |
| Stable time                                       | tCFS        | Fig.4 fo=400kHz<br>Fig.4 fo=800kHz, 1MHz, 4MHz,<br>1/3 predivider, 1/4 predivider<br>VDD=4 to 6V  |  |                           |                            | 10<br>10                   | ms<br>ms                 |
|   |             |   |  |                           |                            |                            |                          |
| 2-pin RC oscillation Frequency                    | fMOSC       | Fig.2 Cext=220pF $\pm 5\%$<br>Fig.2 Rext=4.7k $\Omega$ $\pm 1\%$<br>VDD=4 to 6V   | OSC1, OSC2   | 646                       | 850                        | 1117                       | kHz                      |
|   |             | Fig.2 Cext=220pF $\pm 5\%$<br>Fig.2 Rext=12k $\Omega$ $\pm 1\%$<br>VDD=3 to 6V  | OSC1, OSC2   | 304                       | 400                        | 580                        | kHz                      |

| Parameter   | Symbol | Conditions                                   | Pins            | Limits |            |      |            |
|---|--------|--|-----------------|--------|------------|------|------------|
|   |        |  |                 | min.   | typ.       | max. | unit       |
| Pull-up resistance<br>I/O port pull-up resistance | RPP    | VDD=5V                                       | Port of PU type |        | 14         |      | k $\Omega$ |
| External reset characteristics<br>Reset time      | tRST   |  |                 |        | See Fig.5. |      |            |
| Pin capacitance                                   | Cp     | f=1MHz Other than pins to be tested, VIN=VSS |                 |        | 10         |      | pF         |

- (\*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.
- (\*2) Average over the period of 100ms.
- (\*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
- (\*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.
- (\*5) fCOSC: oscillation frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

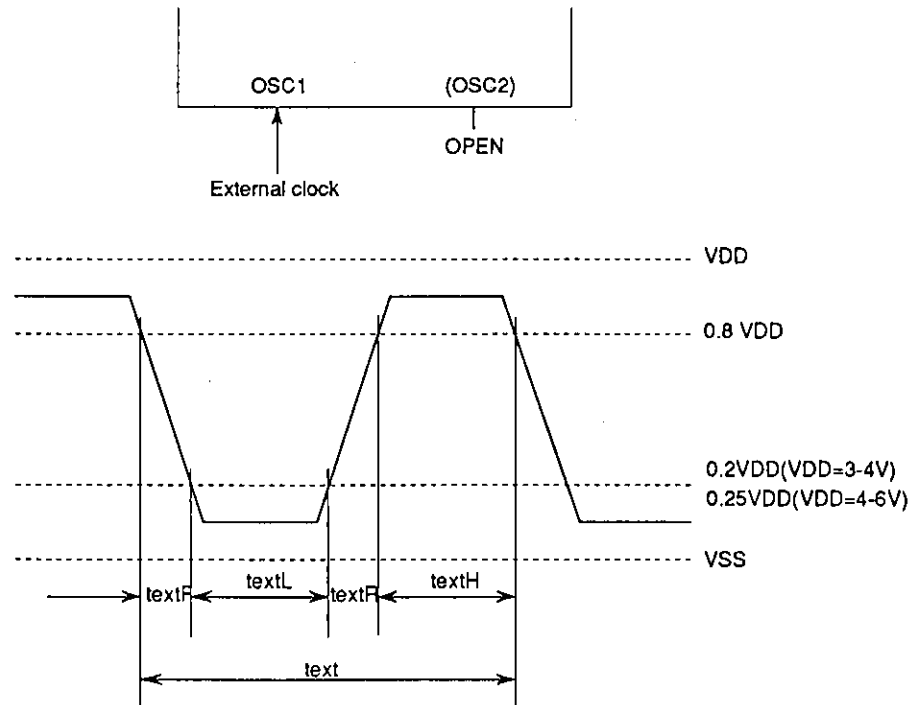


Fig. 1 External Clock Input Waveform

\* External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

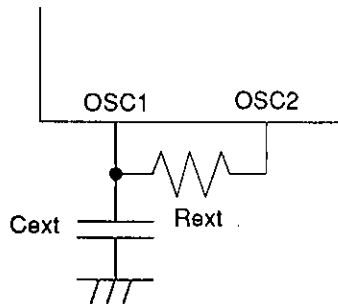


Fig. 2 2-pin RC Oscillation Circuit

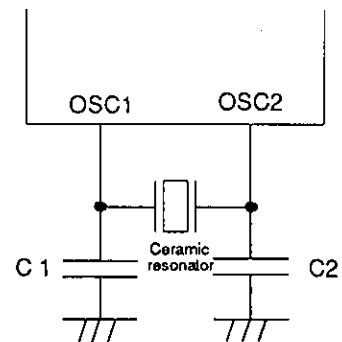


Fig. 3 Ceramic Resonator Oscillation Circuit

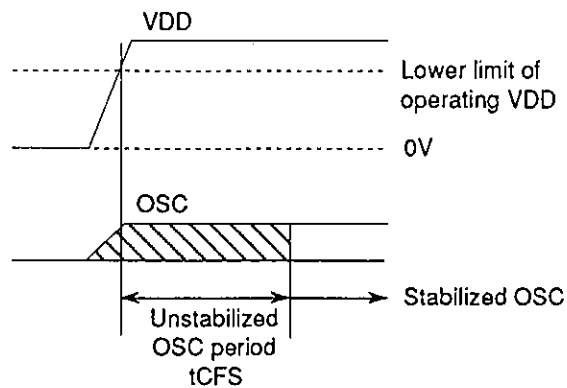


Fig. 4 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for  
Ceramic Resonator OSC

|   |    |           |
|---|----|-----------|
| 4MHz (Murata)<br>CSA4.00MG                            | C1 | 33pF±10%  |
|   | C2 | 33pF±10%  |
|   | R  | 0Ω        |
| 4MHz (Kyocera)<br>KBR4.0MSA<br>KBR4.0MKS (built-in C) | C1 | 33pF±10%  |
|   | C2 | 33pF±10%  |
|   | R  | 0Ω        |
| 1MHz (Murata)<br>CSB1000J                             | C1 | 100pF±10% |
|   | C2 | 100pF±10% |
|   | R  | 2.2kΩ     |
| 1MHz (Kyocera)<br>KBR1000F                            | C1 | 100pF±10% |
|   | C2 | 100pF±10% |
|   | R  | 0Ω        |
| 800kHz (Murata)<br>CSB800J                            | C1 | 100pF±10% |
|   | C2 | 100pF±10% |
|   | R  | 2.2kΩ     |
| 800kHz (Kyocera)<br>KBR800F                           | C1 | 100pF±10% |
|   | C2 | 100pF±10% |
|   | R  | 0Ω        |
| 400kHz (Murata)<br>CSB400P                            | C1 | 220pF±10% |
|   | C2 | 220pF±10% |
|   | R  | 2.2kΩ     |
| 400kHz (Kyocera)<br>KBR400BK                          | C1 | 330pF±10% |
|   | C2 | 330pF±10% |
|   | R  | 0Ω        |

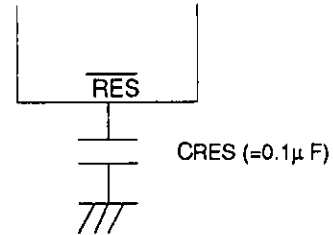


Fig. 5 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at  $C_{RES}=0.1\mu F$ . If the rise time of the power supply is long, the value of  $C_{RES}$  must be increased so that the reset time becomes 10ms or more.



## RC Oscillation Characteristics of the LC6527N, LC6528N

Fig. 6 shows the RC oscillation characteristics of the LC6527N, 6528N. For the variation range of RC OSC frequency of the LC6527N, LC6528N, the following are guaranteed at the external constants only shown below.

- 1)  $V_{DD}=3.0V$  to  $6.0V$ ,  $T_a=-40^{\circ}C$  to  $+85^{\circ}C$   
 External constants       $C_{ext} = 220 \text{ pF}$   
                                   $R_{ext} = 12 \text{ k}\Omega$   
                                   $304 \text{ kHz} \leq f_{MOSC} \leq 580 \text{ kHz}$
- 2)  $V_{DD}=4.0V$  to  $6.0V$ ,  $T_a=-40^{\circ}C$  to  $+85^{\circ}C$   
                                   $C_{ext} = 220 \text{ pF}$   
                                   $R_{ext} = 4.7 \text{ k}\Omega$   
                                   $646 \text{ kHz} \leq f_{MOSC} \leq 1117 \text{ kHz}$

If any other constants than specified above are used, the range of  $R_{ext}=3\text{k}\Omega$  to  $20\text{k}\Omega$ ,  $C_{ext}=150\text{pF}$  to  $390\text{pF}$  must be observed. (See Fig.6.)

(\*6) : The oscillation frequency at  $V_{DD}=5.0V$ ,  $T_a=+25^{\circ}C$  must be in the range of  $350\text{kHz}$  to  $750\text{kHz}$ .

(\*7) : The oscillation frequency at  $V_{DD}=4.0$  to  $6.0V$ ,  $T_a=-40^{\circ}C$  to  $+85^{\circ}C$  and  $V_{DD}=3.0V$  to  $6.0V$ ,  $T_a=-40^{\circ}C$  to  $85^{\circ}C$  must be within the operation clock frequency range.

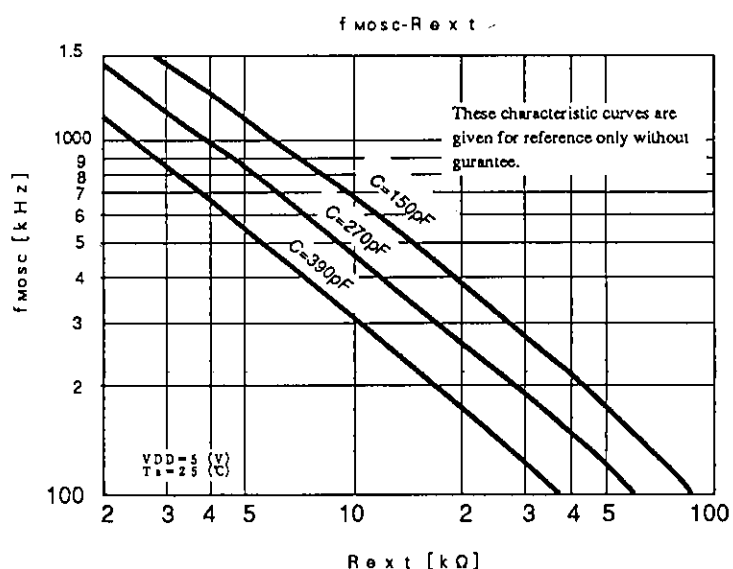


Fig. 6 RC Oscillation Frequency Data (Typ.)

## LC6527F, LC6528F

## 1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

| Parameter                   | Symbol    | Conditions                                    | Pin                      | Limits                            | unit |
|-----------------------------|-----------|---|--------------------------|-----------------------------------|------|
| Maximum supply voltage      | VDD max   |   | VDD                      | -0.3 to +7.0                      | V    |
| Output voltage              | VO        |   | OSC2                     | Allowable up to voltage generated | V    |
| Input voltage               | VI(1)     |   | OSC1 (*1)                | -0.3 to VDD+0.3                   | V    |
|                             | VI(2)     |   | TEST, RES                | -0.3 to VDD+0.3                   | V    |
| Input/output voltage        | VIO(1)    |   | Port of OD type          | -0.3 to +15                       | V    |
|                             | VIO(2)    |   | Port of PU type          | -0.3 to VDD+0.3                   | V    |
| Peak output current         | IOP       |   | I/O Port                 | -2 to +20                         | mA   |
| Average output current      | IOA       | Per pin over the period of 100ms              | I/O Port                 | -2 to +20                         | mA   |
|                             | ΣIOA(1)   | Total current of PA0 to 3, (*2)               | PA0 to 3                 | -6 to +40                         | mA   |
|                             | ΣIOA(2)   | Total current of PC0 to 3, PD0 to 3, PH0 (*2) | PC0 to 3 PH0<br>PD0 to 3 | -14 to +90                        | mA   |
| Allowable power dissipation | Pd max(1) | Ta=-40 to +85°C (DIP package)                 |                          | 250                               | mW   |
|                             | Pd max(2) | Ta=-40 to +85°C (MFP package)*                |                          | 150                               | mW   |
| Operating temperature       | Topg      |   |                          | -40 to +85                        | °C   |
| Storage temperature         | Tstg      |   |                          | -55 to +125                       | °C   |

\* ..... Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

## 2. Allowable Operating Conditions at Ta=-40 to +85°C, VSS=0V, VDD=4.5 to 6.0V

| Parameter                | Symbol | Conditions              | Pin                         | Limits |      |       |      |
|--------------------------|--------|-------------------------|-----------------------------|--------|------|-------|------|
|                          |        |                         |                             | min.   | typ. | max.  | unit |
| Operating supply voltage | VDD    |                         | VDD                         | 4.5    |      | 6.0   | V    |
| Standby supply voltage   | VST    | RAM, register hold (*3) | VDD                         | 1.8    |      | 6.0   | V    |
| "H"-level input voltage  | VIH(1) | Output Nch Tr. OFF      | Port of OD type (except H0) | 0.7VDD |      | +13.5 | V    |
|                          | VIH(2) | Output Nch Tr. OFF      | Port of PU type (except H0) | 0.7VDD |      | VDD   | V    |
|                          | VIH(3) | Output Nch Tr. OFF      | H0 of OD type               | 0.8VDD |      | +13.5 | V    |
|                          | VIH(4) | Output Nch Tr. OFF      | H0 of PU type               | 0.8VDD |      | VDD   | V    |
|                          | VIH(5) |                         | RES                         | 0.8VDD |      | VDD   | V    |
|                          | VIH(6) | External clock mode     | OSC1                        | 0.8VDD |      | VDD   | V    |

| Parameter   | Symbol        | Conditions          | Pin                     | Limits       |      |                |                   |
|---|---------------|---------------------|-------------------------|--------------|------|----------------|-------------------|
|   |               |                     |                         | min.         | typ. | max.           | unit              |
| "L"-level input voltage                                   | VIL(1)        | Output Nch Tr. OFF  | Port                    | VSS          |      | 0.3VDD         | V                 |
|   | VIL(2)        | External clock mode | OSC1                    | VSS          |      | 0.25VDD        | V                 |
|   | VIL(3)        |                     | TEST                    | VSS          |      | 0.3VDD         | V                 |
|   | VIL(4)        |                     | $\overline{\text{RES}}$ | VSS          |      | 0.25VDD        | V                 |
| Operating frequency<br>(Cycle time)                       | fOP<br>(Tcyc) |                     |                         | 200<br>(20)  |      | 4330<br>(0.92) | kHz<br>( $\mu$ s) |
| External clock conditions                                 |               |                     |                         |              |      |                |                   |
| Frequency   | text          | Fig. 1              | OSC1                    | 200          |      | 4330           | kHz               |
| Pulse width   | textH, textL  |                     | OSC1                    | 69           |      |                | ns                |
| Rise/fall time  | textR, textF  |                     | OSC1                    |              |      | 50             | ns                |
| Oscillation guaranteed constants<br>ceramic resonator OSC |               | Fig. 2              |                         | See Table 1. |      |                |                   |

## 3. Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=4.5 to 6.0V

| Parameter                | Symbol | Conditions  | Pin   | Limits  |        |      |         |
|--------------------------|--------|---|---|---------|--------|------|---------|
|                          |        |   |   | min.    | typ.   | max. | unit    |
| "H"-level input current  | IIH(1) | Output Nch Tr. OFF<br>(including OFF leak current of Nch Tr.)<br>VIN=+13.5V | Port of OD type   |         |        | +5.0 | $\mu$ A |
|                          | IIH(2) | External clock mode,<br>VIN=VDD   | OSC1  |         |        | +1.0 | $\mu$ A |
| "L"-level input current  | IIL(1) | Output Nch Tr. OFF<br>VIN=VSS   | Port of OD type   | -1.0    |        |      | $\mu$ A |
|                          | IIL(2) | Output Nch Tr. OFF<br>VIN=VSS   | Port of PU type   | -1.3    | -0.35  |      | mA      |
|                          | IIL(3) | VIN=VSS   | $\overline{\text{RES}}$                                   | -45     | -10    |      | $\mu$ A |
|                          | IIL(4) | External clock mode,<br>VIN=VSS   | OSC1  | -1.0    |        |      | $\mu$ A |
| "H"-level output voltage | VOH(1) | IOH=-50 $\mu$ A   | Port of PU type   | VDD-1.2 |        |      | V       |
|                          | VOH(2) | IOH=-10 $\mu$ A   | Port of PU type   | VDD-0.5 |        |      | V       |
| "L"-level output voltage | VOL(1) | IOL=10mA  | Port  |         |        | 1.5  | V       |
|                          | VOL(2) | IOL=1.8mA, IOL of each<br>port : 1mA or less                                | Port  |         |        | 0.4  | V       |
| Hysteresis voltage       | VHIS   |   | $\overline{\text{RES}}$ ,<br>OSC1 of schmitt<br>type (*4) |         | 0.1VDD |      | V       |

| Parameter  | Symbol   | Conditions  | Pin             | Limits |             |      |      |
|--|----------|---|-----------------|--------|-------------|------|------|
|  |          |   |                 | min.   | typ.        | max. | unit |
| Current dissipation<br>Ceramic resonator OSC<br>External clock | IDDOP(1) | Fig. 2 4MHz   | VDD             |        | 1.5         | 3.5  | mA   |
|  | IDDOP(2) | 200kHz to 4330kHz<br>*1 Output Nch Tr. OFF at<br>Operating mode<br>Port=VDD | VDD             |        | 1.5         | 3.5  | mA   |
|  | IDDst    | Output Nch Tr. OFF<br>Port=VDD  | VDD             |        | 0.05        | 10   | μA   |
| Standby mode   |          | VDD=6V  | VDD             |        | 0.025       | 5    | μA   |
|  |          | VDD=3V  | VDD             |        |             |      |      |
|  |          |   |                 |        |             |      |      |
| Oscillation characteristics                                    |          |   |                 |        |             |      |      |
| Ceramic resonator OSC  |          |   |                 |        |             |      |      |
| Frequency  | fCFOSC   | Fig.2 fo=4MHz (*5)  | OSC1, OSC2      | 3840   | 4000        | 4160 | kHz  |
| Stable time  | tCFS     | Fig.3 fo=4MHz   |                 |        |             | 10   | ms   |
| Pull-up resistance   |          |   |                 |        |             |      |      |
| I/O port pull-up resistance                                    | RPP      | VDD=5V  | Port of PU type |        | 14          |      | kΩ   |
| External reset characteristics                                 |          |   |                 |        |             |      |      |
| Reset time   | tRST     |   |                 |        | See Fig. 4. |      |      |
| Pin capacitance  | Cp       | f=1MHz, other than pins to be tested, VIN=VSS                               |                 |        | 10          |      | pF   |

(\*1) When oscillated internally under the oscillating conditions in Fig.2, up to the oscillation amplitude generated is allowable.

(\*2) Average over the period of 100ms.

(\*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.

(\*4) The OSC1 pin can be schmitt-triggered when the external clock oscillation option has been selected.

(\*5) fCFOSC : Oscillatable frequency.

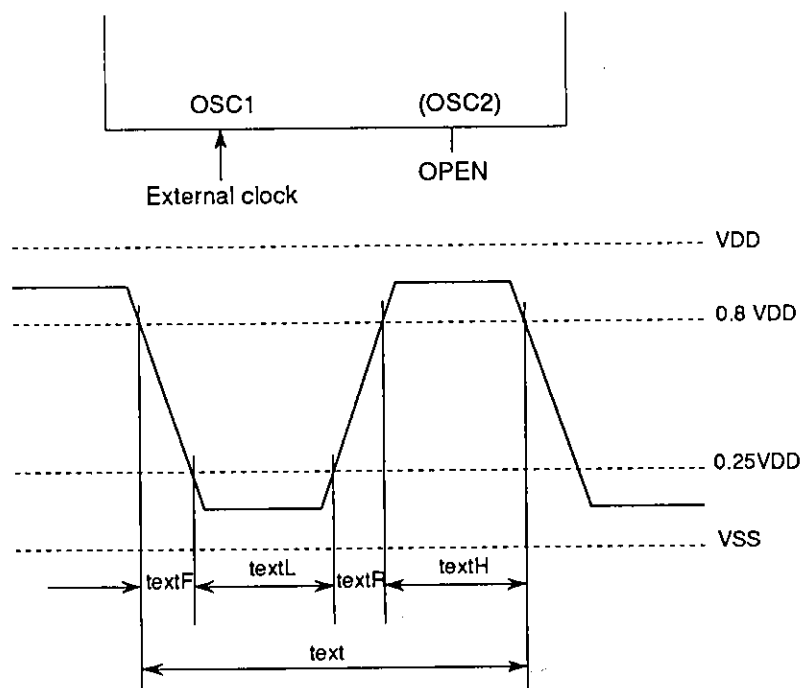


Fig. 1 External Clock Input Waveform

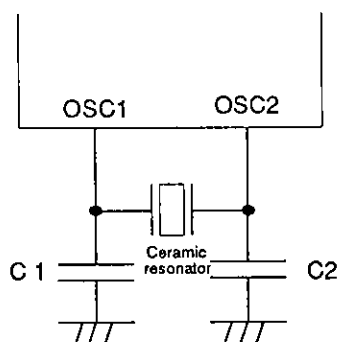


Fig. 2 Ceramic resonator OSC circuit

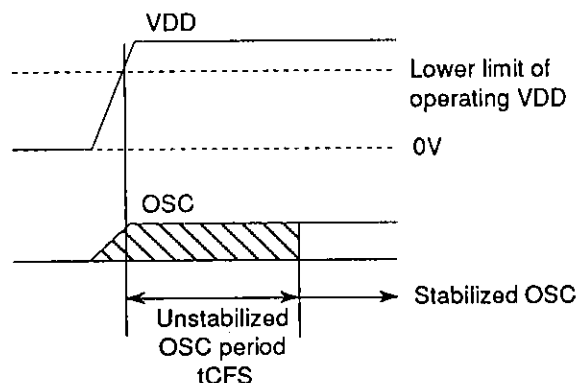


Fig. 3 OSC Stabilizing Period

Table 1. Constants Guaranteed for Ceramic Resonator OSC

|                         |    |                |
|-------------------------|----|----------------|
| 4MHz (Murata)           | C1 | 33pF $\pm$ 10% |
| CSA4.00MG               | C2 | 33pF $\pm$ 10% |
| CST4.00MGW (built-in C) | R  | 0 $\Omega$     |
| 4MHz (Kyocera)          | C1 | 33pF $\pm$ 10% |
| KBR4.0MSA               | C2 | 33pF $\pm$ 10% |
| KBR4.0MKS (built-in C)  | R  | 0 $\Omega$     |

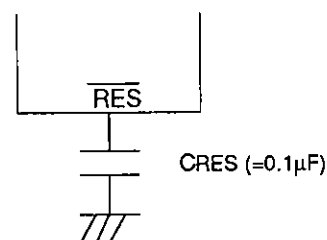


Fig. 4 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at CRES=0.1 $\mu$ F. If the rise time of the power supply is long, the value of CRES must be increased so that the reset time becomes 10ms or more.

## LC6527L, LC6528L

## 1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

| Parameter                   | Symbol                | Conditions                                    | Pin                           | Limits                            | unit |
|-----------------------------|-----------------------|---|-------------------------------|-----------------------------------|------|
| Maximum supply voltage      | VDD max               |   | VDD                           | -0.3 to 7.0                       | V    |
| Output voltage              | VO                    |   | OSC2                          | Allowable up to voltage generated | V    |
| Input voltage               | VI(1)                 |   | OSC1 (*1)                     | -0.3 to VDD+0.3                   | V    |
|                             | VI(2)                 |   | TEST, $\overline{\text{RES}}$ | -0.3 to VDD+0.3                   | V    |
| Input/output voltage        | VIO(1)                |   | Port of OD type               | -0.3 to +15                       | V    |
|                             | VIO(2)                |   | Port of PU type               | -0.3 to VDD+0.3                   | V    |
| Peak output current         | IOP                   |   | I/O Port                      | -2 to +20                         | mA   |
| Average output current      | IOA                   | Per pin over the period of 100ms              | I/O Port                      | -2 to +20                         | mA   |
|                             | $\Sigma\text{IOA}(1)$ | Total current of PA0 to 3, (*2)               | PA0 to 3                      | -6 to +40                         | mA   |
|                             | $\Sigma\text{IOA}(2)$ | Total current of PC0 to 3, PD0 to 3, PH0 (*2) | PC0 to 3 PH0<br>PD0 to 3      | -14 to +90                        | mA   |
| Allowable power dissipation | Pd max(1)             | Ta=-40 to +85°C (DIP package)                 |                               | 250                               | mW   |
|                             | Pd max(2)             | Ta=-40 to +85°C (MFP package)*                |                               | 150                               | mW   |
| Operating temperature       | Topr                  |   |                               | -40 to +85                        | °C   |
| Storage temperature         | Tstg                  |   |                               | -55 to +125                       | °C   |

\* ..... Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

## 2. Allowable Operating Conditions at Ta=-40°C to 85°C, VSS=0V, VDD=2.2 to 6.0V

| Parameter                | Symbol | Conditions              | Pin                         | Limits |      |         |      |
|--------------------------|--------|-------------------------|-----------------------------|--------|------|---------|------|
|                          |        |                         |                             | min.   | typ. | max.    | unit |
| Operating supply voltage | VDD    |                         | VDD                         | 2.2    |      | 6.0     | V    |
| Standby supply voltage   | VST    | RAM, register hold (*3) | VDD                         | 1.8    |      | 6.0     | V    |
| "H"-level input voltage  | VIH(1) | Output Nch Tr. OFF      | Port of OD type (except H0) | 0.7VDD |      | +13.5   | V    |
|                          | VIH(2) | Output Nch Tr. OFF      | Port of PU type (except H0) | 0.7VDD |      | VDD     | V    |
|                          | VIH(3) | Output Nch Tr. OFF      | H0 of OD type               | 0.8VDD |      | +13.5   | V    |
|                          | VIH(4) | Output Nch Tr. OFF      | H0 of PU type               | 0.8VDD |      | VDD     | V    |
|                          | VIH(5) |                         | $\overline{\text{RES}}$     | 0.8VDD |      | VDD     | V    |
|                          | VIH(6) | External clock          | OSC1                        | 0.8VDD |      | VDD     | V    |
| "L"-level input voltage  | VIL(1) | Output Nch Tr. OFF      | Port                        | VSS    |      | 0.2VDD  | V    |
|                          | VIL(2) | External clock          | OSC1                        | VSS    |      | 0.15VDD | V    |
|                          | VIL(3) |                         | TEST                        | VSS    |      | 0.2VDD  | V    |
|                          | VIL(4) |                         | $\overline{\text{RES}}$     | VSS    |      | 0.2VDD  | V    |

| Parameter                        | Symbol       | Conditions  | Pin        | Limits   |      |              |          |
|----------------------------------|--------------|---|------------|----------|------|--------------|----------|
|                                  |              |   |            | min.     | typ. | max.         | unit     |
| Operating frequency (cycle time) | fOP (Tcyc)   | When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.16MHz. |            | 200 (20) |      | 1040 (3.84)  | kHz (μs) |
| External Clock conditions        |              |   |            |          |      |              |          |
| Frequency                        | text         | Fig.1 When clock exceeds 1.040MHz, the 1/3 or 1/4 predivider option is selected.  | OSC1       | 200      |      | 4160         | kHz      |
| Pulse width                      | textH, textL |   | OSC1       | 100      |      |              | ns       |
| Rise/fall time                   | textR, textF |   | OSC1       |          |      | 100          | ns       |
| Oscillation guaranteed constants |              |   |            |          |      |              |          |
| 2-pin RC oscillation             | Cext         | Fig.2   | OSC1, OSC2 |          |      | 220 ± 5%     | pF       |
|                                  | Rext         |   |            |          |      | 12 ± 1%      | kΩ       |
| Ceramic oscillation              |              | Fig.3   |            |          |      | See Table 1. |          |

### 3. Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=2.2 to 6.0V

| Parameter                | Symbol              | Conditions   | Pin                            | Limits  |        |      |      |
|--------------------------|---------------------|--|--------------------------------|---------|--------|------|------|
|                          |                     |  |                                | min.    | typ.   | max. | unit |
| "H"-level input current  | I <sub>IH</sub> (1) | Output Nch Tr. OFF (including OFF leak current of Nch Tr.)<br>VIN=+13.5V | Port of OD type                |         |        | +5.0 | μA   |
|                          | I <sub>IH</sub> (2) | External clock mode,<br>VIN=VDD  | OSC1                           |         |        | +1.0 | μA   |
| "L"-level input current  | I <sub>IL</sub> (1) | Output Nch Tr. OFF<br>VIN=VSS  | Port of OD type                | -1.0    |        |      | μA   |
|                          | I <sub>IL</sub> (2) | Output Nch Tr. OFF<br>VIN=VSS  | Port of PU type                | -1.3    | -0.35  |      | mA   |
|                          | I <sub>IL</sub> (3) | VIN=VSS  | RES                            | -45     | -10    |      | μA   |
|                          | I <sub>IL</sub> (4) | External clock mode,<br>VIN=VSS  | OSC1                           | -1.0    |        |      | μA   |
| "H"-level output voltage | VOH                 | IOH=-10μA  | Port of PU type                | VDD-0.5 |        |      | V    |
| "L"-level output voltage | VOL(1)              | IOL=3mA  | Port                           |         |        | 1.5  | V    |
|                          | VOL(2)              | IOL=1mA, IOL of each port:<br>1mA or less                                | Port                           |         |        | 0.4  | V    |
| Hysteresis voltage       | VHIS                |  | RES, OSC1 of Schmitt type (*4) |         | 0.1VDD |      | V    |

| Parameter   | Symbol         | Conditions  | Pin             | Limits      |       |          |          |
|---|----------------|---|-----------------|-------------|-------|----------|----------|
|   |                |   |                 | min.        | typ.  | max.     | unit     |
| Current dissipation<br>2-pin RC OSC<br>Ceramic OSC      | IDDOP(1)       | Output Nch Tr. OFF at operating, Port=VDD<br>Fig.2 fOSC=400kHz (TYP)  | VDD             |             | 0.8   | 2.5      | mA       |
|   | IDDOP(2)       | Fig.3 4MHz, 1/4predivider   | VDD             |             | 1.2   | 2.5      | mA       |
|   | IDDOP(3)       | Fig.3 4MHz, 1/4predivider<br>VDD=2.2V   | VDD             |             | 0.5   | 1        | mA       |
|   | IDDOP(4)       | Fig.3 400kHz  | VDD             |             | 0.5   | 2        | mA       |
|   | IDDOP(5)       | Fig.3 800kHz  | VDD             |             | 1.0   | 2.5      | mA       |
|   | IDDOP(6)       | 200kHz to 667kHz,<br>1/1 predivider<br>600kHz to 2000kHz,<br>1/3 predivider<br>800kHz to 2667kHz,<br>1/4 predivider | VDD             |             | 1.0   | 2.5      | mA       |
| Standby mode  | IDDst          | Output Nch Tr. OFF<br>VDD=6V  | VDD             |             | 0.05  | 10       | μA       |
|   |                | Port=VDD VDD=2.2V   | VDD             |             | 0.025 | 5        | μA       |
| Oscillation characteristics<br>Ceramic OSC<br>Frequency | fCFOSC<br>(*)5 | Fig.3 fo=400kHz   | OSC1, OSC2      | 384         | 400   | 416      | kHz      |
|   |                | Fig.3 fo=800kHz   | OSC1, OSC2      | 768         | 800   | 832      | kHz      |
|   |                | Fig.3 fo=1MHz   | OSC1, OSC2      | 960         | 1000  | 1040     | kHz      |
|   |                | Fig.3 fo=4MHz,<br>1/4 predivider  | OSC1, OSC2      | 3840        | 4000  | 4160     | kHz      |
|   | Stable time    | Fig.4 fo=400kHz<br>Fig.4 fo=800kHz, 1MHz,<br>4MHz, 1/4 predivider   |                 |             |       | 10<br>10 | ms<br>ms |
| 2-pin RC OSC<br>Frequency                               | fMOSC          | Fig.2 Cext=220pF±5%<br>Fig.2 Rext=12kΩ±1%   | OSC1, OSC2      | 281         | 400   | 580      | kHz      |
| Pull-up resistance<br>I/O port pull-up resistance       | RPP            | VDD=5V  | Port of PU type |             | 14    |          | kΩ       |
| External reset characteristics<br>Reset time            | tRST           |   |                 | See Fig. 5. |       |          |          |
| Pin capacitance   | Cp             | f=1MHz, Other than pins to be tested, VIN=VSS   |                 |             | 10    |          | pF       |

(\*)1 When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.

(\*)2 Average over the period of 100ms.

(\*)3 Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.

(\*)4 The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option, or external clock oscillation option has been selected.

(\*)5 fCFOSC : Oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.



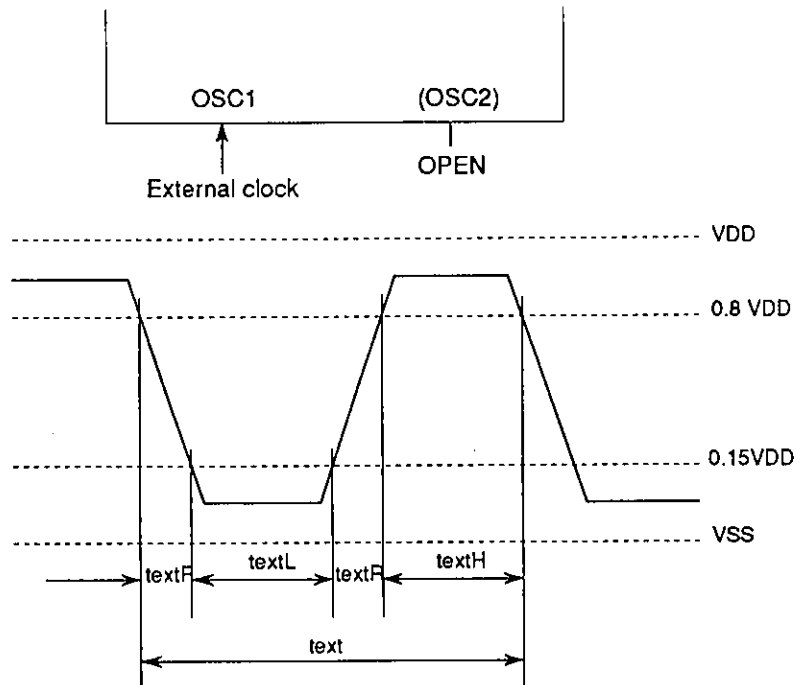


Fig. 1 External Clock Input Waveform

\* External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

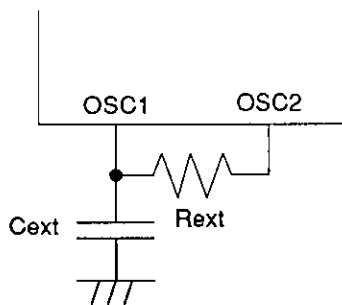


Fig. 2 2-pin RC Oscillation Circuit

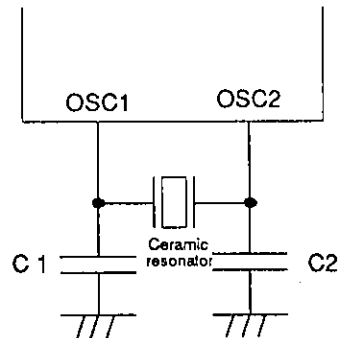


Fig. 3 Ceramic Resonator Oscillation Circuit

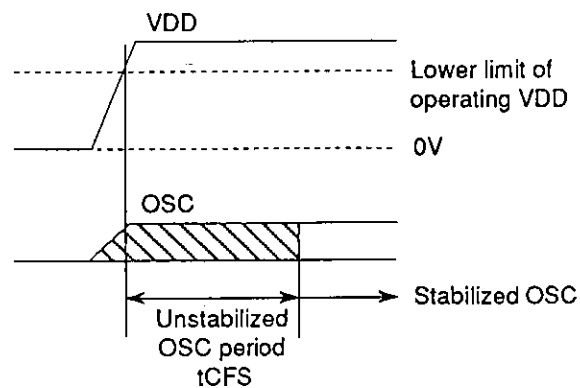


Fig. 4 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for  
Ceramic Resonator OSC

|                              |    |           |
|------------------------------|----|-----------|
| 4MHz (Murata)<br>CSA4.00MGU  | C1 | 33pF±10%  |
|                              | C2 | 33pF±10%  |
|                              | R  | 0Ω        |
| 1MHz (Murata)<br>CSB1000J    | C1 | 100pF±10% |
|                              | C2 | 100pF±10% |
|                              | R  | 2.2kΩ     |
| 1MHz (Kyocera)<br>KBR1000F   | C1 | 100pF±10% |
|                              | C2 | 100pF±10% |
|                              | R  | 0Ω        |
| 800kHz (Murata)<br>CSB800J   | C1 | 100pF±10% |
|                              | C2 | 100pF±10% |
|                              | R  | 2.2kΩ     |
| 800kHz (Kyocera)<br>KBR800F  | C1 | 100pF±10% |
|                              | C2 | 100pF±10% |
|                              | R  | 0Ω        |
| 400kHz (Murata)<br>CSB400P   | C1 | 220pF±10% |
|                              | C2 | 220pF±10% |
|                              | R  | 2.2kΩ     |
| 400kHz (Kyocera)<br>KBR400BK | C1 | 330pF±10% |
|                              | C2 | 330pF±10% |
|                              | R  | 0Ω        |

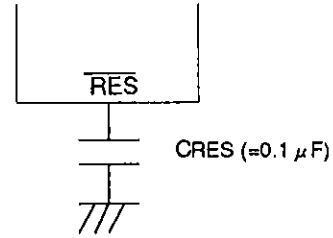


Fig. 5 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at CRES=0.1μF. If the rise time of the power supply is long, the value of CRES must be increased so that the reset time becomes 10ms or more.

## RC Oscillation Characteristic of the LC6527L, 6528L

Fig. 6 shows the RC oscillation characteristic of the LC6527L, 6528L. For the variation range of RC OSC frequency of the LC6527L, 6528L, the following are guaranteed at the external constants only shown below.

VDD=2.2V to 6.0V, Ta=-40°C to +85°C

External constants      Cext = 220 pF

Rext = 12 kΩ

281 kHz ≤ fMOSC ≤ 580 kHz

If any other constants than specified above are used, the range of Rext=3kΩ to 20kΩ, Cext=150pF to 390pF must be observed. (See Fig. 6.)

(\*6) : The oscillation frequency at VDD=5.0V, Ta=+25°C must be in the range of 350kHz to 500kHz.

(\*7) : The oscillation frequency at VDD=2.2 to 6.0V and Ta=-40°C to +85°C must be within the operation clock frequency range.

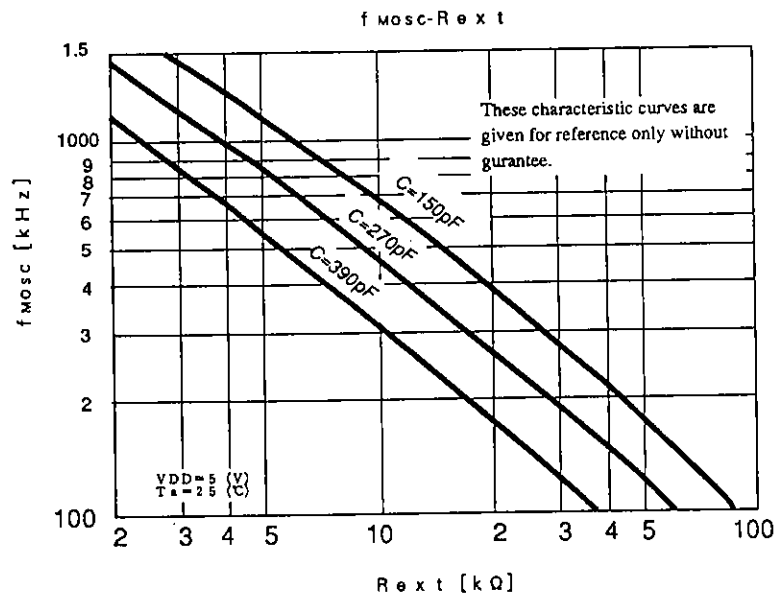


Fig. 6 RC Oscillation Frequency Data (Typ.)

## Notes for Program Evaluation

- When evaluating the LC6527/28 with the evaluation chip (LC6596, LC65PG23/26), the following must be observed.

| Classification   | Item                                  | Function   |  | Notes for evaluation  |
|------------------|---------------------------------------|--|--|---|
|                  |                                       | Mass-production chip   | Evaluation chip  |   |
| Notes for option | 2-pin OSC                             | PH0 and OSC2 share one pin (PH0/OSC2). Either of them is selected exclusively by user option.<br>When 2-pin OSC is selected, PH0/OSC2 pin provides OSC2 and performs no function as PH0 port. Data input to PH0/OSC2 by mistake is always read as "0". | Evaluation chip has PH0 and OSC2 separately. Pin required for option is selected as required. Even when OSC2 pin is selected by option, PH0 circuit is present and functions as complete port PH0. | Since input/output at PH0 on evaluation chip results in difference between evaluation chip operation and mass-production chip operation, input/output at PH0 is prohibited.   |
|                  | OSC predivider                        | 3 selections (1/1, 1/3, 1/4) by option.  | 3 selections (1/1, 1/3, 1/4) available by 2 pins of DIV pin, 3OR4 pin.   | DIV pin, 3OR4 pin must be set according to option specified for mass-production chip.   |
|                  | Ports C, D output level at reset mode | Ports C, D can be brought to "H" or "L" in a group of 4 bits.  | Port C and port D can be brought to "H" and "L" by CHL pin and DHL pin respectively.   | CHL pin and DHL pin must be set according to option specified for mass-production chip.   |
|                  | Port output configuration PU/OD       | PU or OD can be selected bitwise.  | Only OD without PU.  | [LC6596-applied evaluation]<br>External resistor (15kohms) on evaluation board must be connected to necessary port.<br>[Piggyback-applied evaluation]<br>Resistor must be connected to necessary port on application board. |
|                  | PU resistor configuration             | PU resistor brought to Hi-Z (Pch Tr to turn OFF) at "L" output mode.   | PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode.  | For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.  |
| Notes for OSC    | OSC constants -1                      | [2-pin RC OSC]<br>Catalog-guaranteed constants provide OSC at frequency specified in catalog.  | [2-pin RC OSC]<br>Different from mass-production chip in circuit design and characteristic.  | [2-pin RC OSC]<br>Frequency must be adjusted to OSC frequency of mass-production chip by adjusting variable resistor.   |
|                  |                                       | [2-pin ceramic resonator OSC]<br>Catalog-guaranteed constants provide OSC at frequency specified in catalog.   | [2-pin ceramic resonator OSC]<br>Different from mass-production chip in circuit design and characteristic.<br>Wiring capacitance may provide unstable OSC.   | [2-pin ceramic resonator OSC]<br>External constants must be fine-adjusted according to service conditions.  |
|                  | OSC constants -2<br>(Note)            | [2-pin ceramic resonator OSC]<br>Feedback resistor is contained.   | [2-pin ceramic resonator OSC]<br>No feedback resistor is contained.  | [2-pin ceramic resonator OSC]<br>For evaluation chip, feedback resistor of 1Mohm must be connected externally.  |

Continued on next page.

Continued from preceding page.

| Classification                       | Item                               | Function  |   | Notes for evaluation   |
|--------------------------------------|------------------------------------|---|---|--|
|                                      |                                    | Mass-production chip                                  | Evaluation chip   |  |
| Notes for electrical characteristics | OSC frequency                      | OSC frequency characteristic as indicated in catalog. | Different from mass-production chip in circuit design, and characteristic.  | ES, CS must be used to evaluate characteristic in detail.          |
|                                      | Operating current, standby current | Current characteristic as indicated in catalog.       | Different from mass-production chip in circuit design, characteristic.      |  |
| Other notes                          | Type No. setting                   | LC6527/28 differ in ROM, RAM.                         | ROM, RAM to be used according to Type No. are set by INSTC, MEMC.           | INSTC, MEMC are set according to Type No. of mass-production chip. |
|                                      | Evaluation chip pin setting        |   | Input pin RSTC, which is not provided in mass-production chip, is provided. | SW4 on evaluation board must remain turned OFF.                    |

Note) When the evaluation chip is used in the 2-pin ceramic resonator OSC mode, no feedback resistor is contained unlike the mass-production chip. Connect a feedback resistor of 1Mohm externally as shown below. Since constants R, C are also differ from those for the mass-production chip, refer to Table 1 and adjust the capacitor value according to the stray capacitance of the circuit.

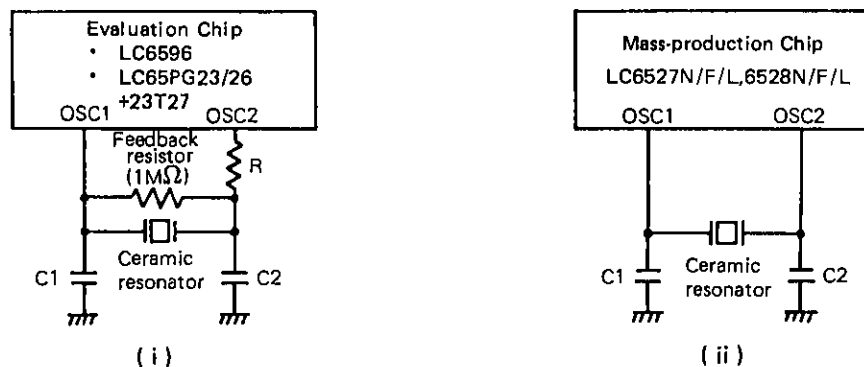


Fig. 1 2-Pin Ceramic Resonator OSC Circuit for Evaluation Chip and Mass-production Chip

| Ceramic resonator |                              | Mass-production chip<br>C1=C2 | Evaluation chip (*)                                 |       |  |       |
|-------------------|------------------------------|-------------------------------|---|-------|--|-------|
|                   |                              |                               | Including capacitance of standard cable(FAS-20-03B) |       | Including no capacitance of standard cable(FAS-20-03B) |       |
|                   |                              |                               | C1=C2   | R     | C1=C2  | R     |
| 4MHz              | CSA4.00MG (Murata)           | 30pF                          | 8pF   | 0Ω    | 33pF   | 0Ω    |
|                   | KBR4.0MS (Kyocera)           | 33pF                          | 8pF   | 0Ω    | 33pF   | 0Ω    |
| 1MHz              | CSB1000K (Murata)            | (Using CSB1000D)<br>100pF     | 82pF  | 2.2kΩ | 100pF  | 2.2kΩ |
|                   | KBR1000H (Kyocera)           | 100pF                         | 82pF  | 2.2kΩ | 100pF  | 2.2kΩ |
| 800kHz            | CSB800K (Murata)             | (Using CSB800D)<br>100pF      | 120pF   | 2.2kΩ | 150pF  | 2.2kΩ |
|                   | KBR800H (Kyocera)            | 100pF                         | 120pF   | 2.2kΩ | 150pF  | 2.2kΩ |
| 400kHz            | CSB400P (Murata)             | 330pF                         | 220pF   | 3.3kΩ | 270pF  | 3.3kΩ |
|                   | KBR400B (Kyocera)<br>KBR400H | 150pF                         | 330pF   | 1.0kΩ | 330pF  | 1.0kΩ |

Table 1 Reference Values of Constants R, C

(\*) Standard cable (FAS-20-03B) is a cable attached to target board EVA-TB6523C/26C/27C/28C.

Table 1 shows two cases where the capacitance of the cable is included and no capacitance of the cable is included.

- Example where the capacitance of the cable is included  
The capacitance of the cable is included when the resonator is connected to the user's application board through the cable from the EVA-TB6523C/26C/27C/28C.
- Example where no capacitance of the cable is included  
No capacitance of the cable is included when the resonator is placed near the evaluation chip (on the EVA-TB6523C/26C/27C/28C).

When using any other cable than the attached cable, adjust the capacitor value according to the stray capacitance.

## LC6527, 6528 INSTRUCTION SET (BY FUNCTION)

Symbol Description  
 AC : Accumulator  
 ACt : Accumulator bit t  
 CF : Carry flag  
 DP : Data pointer  
 E : E register  
 M : Memory  
 M(DP) : Memory addressed by DP

P(DP<sub>L</sub>) : Input/output port addressed by DP<sub>L</sub>  
 PC : Program counter  
 STACK : Stack register  
 TM : Timer  
 TMF : Timer (internal) interrupt request flag  
 ZF : Zero flag

( ), ( ) : Contents  
 ← : Transfer and direction  
 + : Addition  
 - : Subtraction  
 ∨ : Exclusive OR

| Instruction group  | Mnemonic          |   | Instruction code   |  | Bytes | Cycles | Function  | Description   | Status flag affected | Remarks |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|--|-------------------|---|--|--|-------|--------|---|---|----------------------|---------|--|----|----|--|--|--|---|---|--|--|--|---|---|--|--|--|---|---|-------|--|
|  |                   |   | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>            | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>                                      |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| Accumulator manipulation instructions                              | CLA               | Clear AC  | 1 1 0 0  | 0 0 0 0  | 1     | 1      | AC ← 0  | The AC contents are cleared.  | ZF                   | * 1     |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | CLC               | Clear CF  | 1 1 1 0  | 0 0 0 1  | 1     | 1      | CF ← 0  | The CF contents are cleared.  | CF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | STC               | Set CF  | 1 1 1 1  | 0 0 0 1  | 1     | 1      | CF ← 1  | The CF is set.  | CF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | CMA               | Complement AC   | 1 1 1 0  | 1 0 1 1  | 1     | 1      | AC ← $\overline{AC}$  | The AC contents are complemented.   | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | INC               | Increment AC  | 0 0 0 0  | 1 1 1 0  | 1     | 1      | AC ← (AC) + 1   | The AC contents are incremented +1.   | ZF CF                |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | DEC               | Decrement AC  | 0 0 0 0  | 1 1 1 1  | 1     | 1      | AC ← (AC) - 1   | The AC contents are decremented -1.   | ZF CF                |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | TAE               | Transfer AC to E  | 0 0 0 0  | 0 0 1 1  | 1     | 1      | E ← (AC)  | The AC contents are transferred to the E.   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | XAE               | Exchange AC with E  | 0 0 0 0  | 1 1 0 1  | 1     | 1      | (AC) ↔ (E)  | The AC contents and the E contents are exchanged.   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| Memory manipulation instructions                                   | INM               | Increment M   | 0 0 1 0  | 1 1 1 0  | 1     | 1      | M(DP) ← (M(DP)) + 1   | The M(DP) contents are incremented +1.  | ZF CF                |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | DEM               | Decrement M   | 0 0 1 0  | 1 1 1 1  | 1     | 1      | M(DP) ← (M(DP)) - 1   | The M(DP) contents are decremented -1.  | ZF CF                |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | SMB bit           | Set M data bit  | 0 0 0 0  | 1 0 B <sub>1</sub> B <sub>0</sub>  | 1     | 1      | M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1   | A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is set.  |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | RMB bit           | Reset M data bit  | 0 0 1 0  | 1 0 B <sub>1</sub> B <sub>0</sub>  | 1     | 1      | M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0   | A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is reset.  | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| Arithmetic operation/comparison instructions                       | AD                | Add M to AC   | 0 1 1 0  | 0 0 0 0  | 1     | 1      | AC ← (AC) + (M(DP))   | Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.  | ZF CF                |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | ADC               | Add M to AC with CF   | 0 0 1 0  | 0 0 0 0  | 1     | 1      | AC ← (AC) + (M(DP)) + (CF)  | Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.  | ZF CF                |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | DAA               | Decimal adjust AC in addition   | 1 1 1 0  | 0 1 1 0  | 1     | 1      | AC ← (AC) + 6   | 6 is added to the AC contents.  | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | DAS               | Decimal adjust AC in subtraction  | 1 1 1 0  | 1 0 1 0  | 1     | 1      | AC ← (AC) + 10  | 10 is added to the AC contents.   | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | EXL               | Exclusive or M to AC  | 1 1 1 1  | 0 1 0 1  | 1     | 1      | AC ← (AC) ∨ (M(DP))   | The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.   | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | CM                | Compare AC with M   | 1 1 1 1  | 1 0 1 1  | 1     | 1      | (M(DP)) + (AC) + 1  | The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset.<br><table><tr><th colspan="3">Comparison result</th><th>CF</th><th>ZF</th></tr><tr><td>(M(DP)) &gt; (AC)</td><td></td><td></td><td>0</td><td>0</td></tr><tr><td>(M(DP)) = (AC)</td><td></td><td></td><td>1</td><td>1</td></tr><tr><td>(M(DP)) &lt; (AC)</td><td></td><td></td><td>1</td><td>0</td></tr></table>  | Comparison result    |         |  | CF | ZF | (M(DP)) > (AC)   |  |  | 0 | 0 | (M(DP)) = (AC)   |  |  | 1 | 1 | (M(DP)) < (AC)   |  |  | 1 | 0 | ZF CF |  |
| Comparison result  |                   |   | CF   | ZF   |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| (M(DP)) > (AC)   |                   |   | 0  | 0  |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| (M(DP)) = (AC)   |                   |   | 1  | 1  |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| (M(DP)) < (AC)   |                   |   | 1  | 0  |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| Load/store instructions  | CI data           | Compare AC with immediate data  | 0 0 1 0<br>0 1 0 0   | 1 1 0 0<br>1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub>                           | 2     | 2      | 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> + (AC) + 1  | The AC contents and the immediate data 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> are compared and the ZF and CF are set/reset.<br><table><tr><th colspan="3">Comparison result</th><th>CF</th><th>ZF</th></tr><tr><td>1<sub>3</sub>1<sub>2</sub>1<sub>1</sub>1<sub>0</sub> &gt; (AC)</td><td></td><td></td><td>0</td><td>0</td></tr><tr><td>1<sub>3</sub>1<sub>2</sub>1<sub>1</sub>1<sub>0</sub> = (AC)</td><td></td><td></td><td>1</td><td>1</td></tr><tr><td>1<sub>3</sub>1<sub>2</sub>1<sub>1</sub>1<sub>0</sub> &lt; (AC)</td><td></td><td></td><td>1</td><td>0</td></tr></table> | Comparison result    |         |  | CF | ZF | 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> > (AC) |  |  | 0 | 0 | 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> = (AC) |  |  | 1 | 1 | 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> < (AC) |  |  | 1 | 0 | ZF CF |  |
|  | Comparison result |   |  | CF   | ZF    |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> > (AC) |                   |   | 0  | 0  |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> = (AC) |                   |   | 1  | 1  |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> < (AC) |                   |   | 1  | 0  |       |        |   |   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| Data pointer manipulation instructions                             | LI data           | Load AC with immediate data   | 1 1 0 0  | 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub>                                      | 1     | 1      | AC ← 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub>  | The immediate data 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> is loaded in the AC.   | ZF                   | * 1     |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | S                 | Store AC to M   | 0 0 0 0  | 0 0 1 0  | 1     | 1      | M(DP) ← (AC)  | The AC contents are stored in the M(DP).  |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | L                 | Load AC from M  | 0 0 1 0  | 0 0 0 1  | 1     | 1      | AC ← (M(DP))  | The M(DP) contents are loaded in the AC.  | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | LDZ data          | Load DP <sub>H</sub> with zero and DP <sub>L</sub> with immediate data respectively | 1 0 0 0  | 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub>                                      | 1     | 1      | DP <sub>H</sub> ← 0<br>DP <sub>L</sub> ← 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub>  | The DP <sub>H</sub> and DP <sub>L</sub> are loaded with 0 and the immediate data 1 <sub>3</sub> 1 <sub>2</sub> 1 <sub>1</sub> 1 <sub>0</sub> respectively.  |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | LHI data          | Load DP <sub>H</sub> with immediate data  | 0 1 0 0  | 0 0 1 1 1 0  | 1     | 1      | DP <sub>H</sub> ← 1 <sub>3</sub> 1 <sub>0</sub>   | The DP <sub>H</sub> is loaded with the immediate data 1 <sub>3</sub> 1 <sub>0</sub> .   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | IND               | Increment DP <sub>L</sub>   | 1 1 1 0  | 1 1 1 0  | 1     | 1      | DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1  | The DP <sub>L</sub> contents are incremented +1.  | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | DED               | Decrement DP <sub>L</sub>   | 1 1 1 0  | 1 1 1 1  | 1     | 1      | DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1  | The DP <sub>L</sub> contents are decremented -1.  | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | TAL               | Transfer AC to DP <sub>L</sub>  | 1 1 1 1  | 0 1 1 1  | 1     | 1      | DP <sub>L</sub> ← (AC)  | The AC contents are transferred to the DP <sub>L</sub> .  |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
| Jump/subroutine instructions                                       | TLA               | Transfer DP <sub>L</sub> to AC  | 1 1 1 0  | 1 0 0 1  | 1     | 1      | AC ← (DP <sub>L</sub> )   | The DP <sub>L</sub> contents are transferred to the AC.   | ZF                   |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | JMP addr          | Jump  | 0 1 1 0<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 0 P <sub>9</sub> P <sub>8</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC ← P <sub>6</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub><br>P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | A jump to the address specified with immediate data P <sub>6</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> occurs.   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | CZP addr          | Call subroutine in the zero page  | 1 0 1 1  | P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                      | 1     | 1      | STACK ← (PC) + 1<br>PC <sub>9~6</sub> ← PC <sub>1~0</sub> ← 0<br>PC <sub>5~2</sub> ← P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>              | A subroutine in page 0 is called.   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | CAL addr          | Call subroutine   | 1 0 1 0<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 0 P <sub>9</sub> P <sub>8</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | STACK ← (PC) + 2<br>PC <sub>9~0</sub> ← P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>              | A subroutine is called.   |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |
|  | RT                | Return from subroutine  | 0 1 1 0  | 0 0 1 0  | 1     | 1      | PC ← (STACK)  | A return from a subroutine occurs.  |                      |         |  |    |    |  |  |  |   |   |  |  |  |   |   |  |  |  |   |   |       |  |

| Instruction group         | Mnemonic  |                       | Instruction code   |  | Bytes | Cycles | Function   | Description  | Status flag affected | Remarks  |
|---------------------------|-----------|-----------------------|--|--|-------|--------|--|--|----------------------|--|
|                           |           |                       | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>            | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>              |       |        |  |  |                      |  |
|                           | BAI addr  | Branch on AC bit      | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 0 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if AC <sub>1</sub> = 1                                      | If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                   |                      | Mnemonic is BAI0 to BAI3 according to the value of t.            |
|                           | BAI addr  | Branch on no AC bit   | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 0 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if AC <sub>1</sub> = 0                                      | If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                   |                      | Mnemonic is BAI0 to BAI3 according to the value of t.            |
|                           | BMI addr  | Branch on M bit       | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 1 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (M(DP <sub>L</sub> .t <sub>1</sub> t <sub>0</sub> )) = 1 | If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                |                      | Mnemonic is BMI0 to BMI3 according to the value of t.            |
|                           | BMI addr  | Branch on no M bit    | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 1 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (M(DP <sub>L</sub> .t <sub>1</sub> t <sub>0</sub> )) = 0 | If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                |                      | Mnemonic is BMI0 to BMI3 according to the value of t.            |
|                           | BPI addr  | Branch on Port bit    | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 0 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (P(DP <sub>L</sub> .t <sub>1</sub> t <sub>0</sub> )) = 1 | If a single bit of port P(DP <sub>L</sub> ) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |                      | Mnemonic is BPI0 to BPI3 according to the value of t.            |
|                           | BPI addr  | Branch on no Port bit | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 0 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (P(DP <sub>L</sub> .t <sub>1</sub> t <sub>0</sub> )) = 0 | If a single bit of port P(DP <sub>L</sub> ) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |                      | Mnemonic is BPI0 to BPI3 according to the value of t.            |
|                           | BTM addr  | Branch on timer       | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if TMF = 1<br>then TMF ← 0                                  | If the TMF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.  | TMF                  |  |
|                           | BNTM addr | Branch on no timer    | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if TMF = 0<br>then TMF ← 0                                  | If the TMF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.  | TMF                  |  |
|                           | BC addr   | Branch on CF          | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 1 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if CF = 1   | If the CF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |                      |  |
|                           | BNC addr  | Branch on no CF       | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 1 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if CF = 0   | If the CF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |                      |  |
|                           | BZ addr   | Branch on ZF          | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if ZF = 1   | If the ZF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |                      |  |
|                           | BNZ addr  | Branch on no ZF       | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC <sub>7</sub> ~0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if ZF = 0   | If the ZF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |                      |  |
| Input/Output instructions | IP        | Input port to AC      | 0 0 0 0  | 1 1 0 0 1  | 1     | 1      | AC ← (P(DP <sub>L</sub> ))   | Port P(DP <sub>L</sub> ) contents are loaded in the AC.  | ZF                   |  |
|                           | OP        | Output AC to port     | 0 1 1 0  | 0 0 0 1 1  | 1     | 1      | P(DP <sub>L</sub> ) ← (AC)   | The AC contents are outputted to port P(DP <sub>L</sub> ).   |                      |  |
|                           | SPB bit   | Set port bit          | 0 0 0 0  | 0 1 B <sub>1</sub> B <sub>0</sub>  | 1     | 2      | P(DP <sub>L</sub> .B <sub>1</sub> B <sub>0</sub> ) ← 1   | A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is set.   |                      | When this instruction is executed, the E contents are destroyed. |
|                           | RPB bit   | Reset port bit        | 0 0 1 0  | 0 1 B <sub>1</sub> B <sub>0</sub>  | 1     | 2      | P(DP <sub>L</sub> .B <sub>1</sub> B <sub>0</sub> ) ← 0   | A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is reset.   | ZF                   | When this instruction is executed, the E contents are destroyed. |
| Other instructions        | WTTM      | Write timer           | 1 1 1 1  | 1 0 0 1 1  | 1     | 1      | TM ← (E). (AC)<br>TMF ← 0  | The E and AC contents are loaded in the timer. The TMF is reset.   | TMF                  |  |
|                           | HALT      | Halt                  | 1 1 1 1  | 0 1 1 0 1  | 1     | 1      | Halt   | All operations stop.   |                      | Only when all pins of port PA are set at L stop.                 |
|                           | NOP       | No operation          | 0 0 0 0  | 0 0 0 0 1  | 1     | 1      | No operation   | No operation is performed, but 1 machine cycle is consumed.  |                      |  |

\*1 If the CLA instruction is used continuously in such a manner as CLA, CLA, -----, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

(The following instructions, which are included in the instruction set of the LC6523, 6526, are excluded.)  
AND, BFn, BI, BNFn, BNI, CLI, JPEA, OR RAL, RCTL, RFB, RTI, RTBL, SCTL, SFB, X, XAH, XA0, XA1, XA2, XA3, XD, XH0, XH1, XI, XL0, XL1, XM



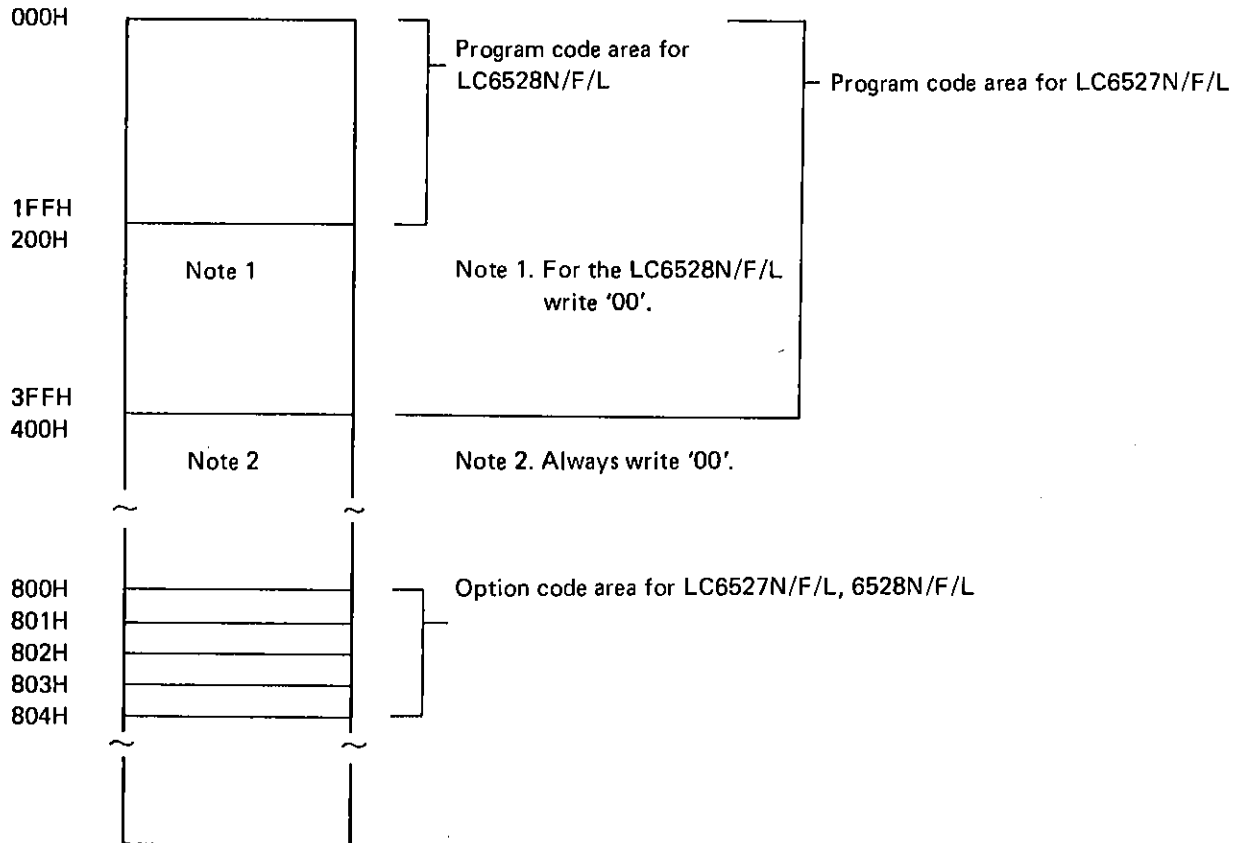
**LC6527N/F/L, 6528N/F/L Option Code Specifying Method****General Description**

It is requested that you should submit to us various mask options of the LC6527N/F/L, LC6528N/F/L together with the program code which are stored in an EPROM.

By using our cross assembler for the LC6527, 6528, the option code can be specified interactively and stored in the EPROM.

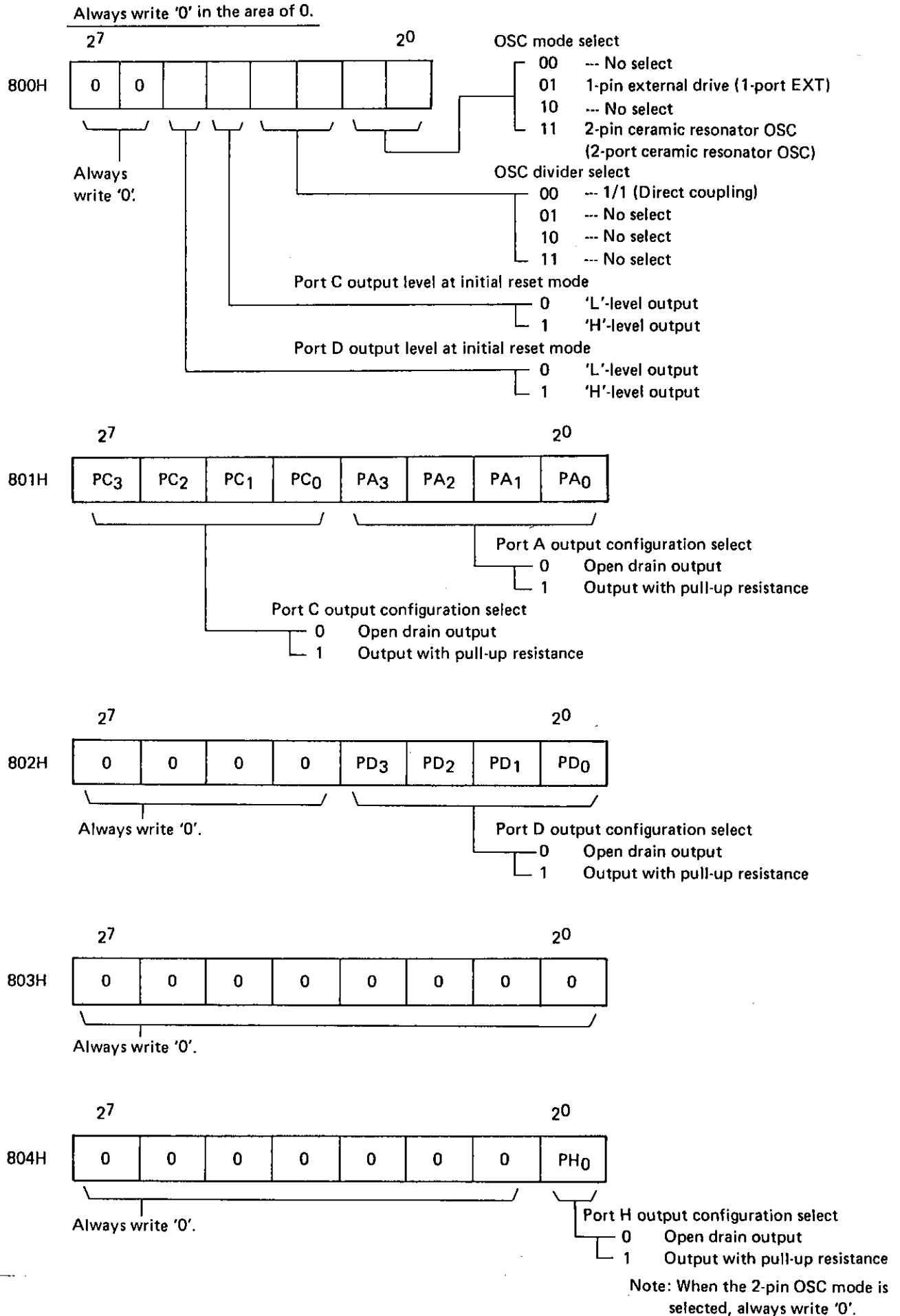
If our cross assembler is not used, specify the option code as shown below. (This is the same as the method where the cross assembler is created automatically.)

The Type No. of the EPROM to be submitted is 2732 or 2764.





H Version (LC6527F, LC6528F) Option Code Specifying Method



## Notes for Standby Function Application

The LC6527N/F/L, 6528N/F/L provide the standby function called HALT mode to minimize the current dissipation when the program is in the wait state.

The standby function is controlled by the HALT instruction, PA pin,  $\overline{\text{RES}}$  pin.

A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed. This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below.

When using the standby function, the application circuit shown below must be used and the notes must be also fully observed.

If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of application equipment.

### 1. HALT mode release conditions

The HALT mode setting, release conditions are shown in Table 1.

Table 1 HALT mode setting, release conditions

| HALT mode setting conditions                    | HALT mode release conditions                                |
|---|---|
| HALT instruction                                | ① Reset (Low level is applied to $\overline{\text{RES}}$ .) |
| Provided that PA <sub>3</sub> is at high level. | ② Low level is applied to PA <sub>3</sub> .                 |

Note) HALT mode release condition ② is available only when the RC mode is used for system clock generation; and unavailable when the ceramic resonator mode is used because the OSC circuit may not operate normally.

### 2. Proper cares in using standby function

When using the standby function, an application circuit and program must be designed with the following in mind.

- (1) The supply voltage at the standby state must not be less than specified.
- (2) Input timing and conditions of each control signal ( $\overline{\text{RES}}$ , PA<sub>3</sub>) must be observed at the standby initiate/release state.
- (3) Release operation must not be overlapped at the time of execution of the HALT instruction.

A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

Sample application where the standby function is used for power failure backup.

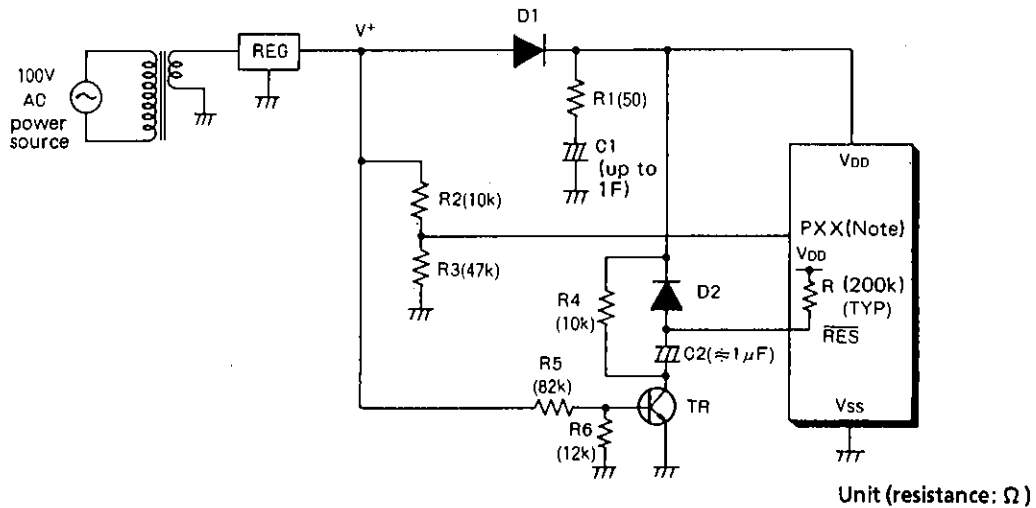
Power failure backup is an application where power failure of the main power source is detected and the HALT instruction is executed to cause the standby state to be entered. The power dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers for a certain period of time. After power is restored, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC). Shown below are sample applications where the program selects or not between power-ON reset and reset after power is restored, notes, measures for instantaneous break of AC power.

## 2-1. Sample application 1 where the standby function is used for power failure backup

Shown below is a sample application where the program does not select between power-ON reset and reset after power is restored.

### 2-1-1. Sample application circuit – (1)

Fig. 2-1 shows a sample application where the standby function is used for power failure backup.



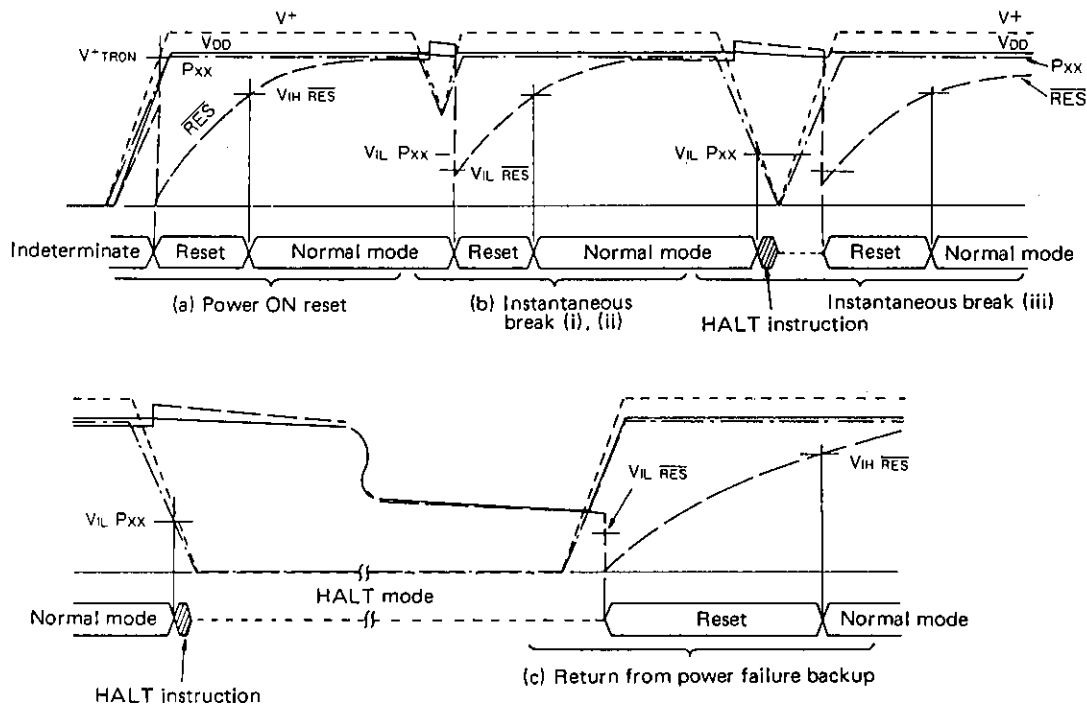
(Note) Normal input ports other than PA3

Fig. 2-1. Sample application – (1) where the standby function is used for power failure backup

### 2-1-2. Operating waveform in sample application circuit – (1)

The operating waveform in the sample application circuit in Fig. 2-1 is shown in Fig. 2-2. The mode is roughly divided as follows:

- (a) Power-ON reset
- (b) Instantaneous break of main power source
- (c) Return from power failure backup



$V^+_{TRON}$ :  $V^+$  value when TR is turned ON/OFF

Fig. 2-2 Operating waveform in sample application circuit – (1)

### 2-1-3. Operation of sample application circuit — (1)

#### (a) At the time of power-ON reset

After power rises, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC).

#### — Note —

This sample application circuit provides an indeterminate region where no reset occurs before the operating  $V_{DD}$  range is entered.

#### (b) At the time of instantaneous break

(i) When the  $P_{XX}$  input voltage does not meet  $V_{IL}$  (the  $P_{XX}$  input level does not get lower than input threshold level  $V_{IL}$ ) and the  $\overline{RES}$  input voltage only meets  $V_{IL}$ :

A reset occurs in the normal mode, providing the same operation as power-ON reset.

(ii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage do not meet  $V_{IL}$ :

The program continues running in the normal mode.

(iii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage meet  $V_{IL}$ :

When two pollings do not regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is not entered and reset occurs.

When two pollings regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode.

#### (c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

### 2-1-4. Notes for design of sample application circuit — (1)

- $V^+$  rise time and C2

Make the time constant (C2, R) of the reset circuit 10 times as long as the  $V^+$  rise time. (R: ON-chip resistor, 200kohms typ.)

Make the  $V^+$  rise time shorter (up to 20ms).

- R1 and C1

Make the R1 value as small as possible. Make the C1 value as large as possible according to the backup time calculated. (Fix the R1 value so that the C1 charging current does not exceed the power source capacity.)

- R2 and R3

Make the "H"-level input voltage applied to the  $P_{XX}$  pin equal to  $V_{DD}$ .

- R4

Fix the time constant of C2 and C4 so that C2 can discharge during the period of time from when  $V^+$  gets lower than  $V^+_{TRON}$  (TR OFF) at the time of instantaneous break until the  $P_{XX}$  input voltage gets lower than  $V_{IL}$  (because release by reset is not available after the HALT mode is entered by instantaneous break).

- R5 and R6

Make  $V^+$  ( $V_{BE} \approx 0.6V$  is obtained by R5 and R6) when the reset circuit works (Tr ON) more than (operating  $V_{DD}$  min +  $V_F$  of diode D1).

Observing this note, make  $V^+$  as low as possible to provide a reset early enough after power-ON.

- Backup time

The normal operation continues with a relatively high current dissipation from when power failure is detected by the  $P_{XX}$  until the HALT instruction is executed. Fix the C1 value so that the standby supply voltage is held during backup time of set + above-mentioned time.

### 2-1-5. Notes for software design

- Design the program so that port A3 is brought to "H" level at the standby mode.

- Check a standby request by polling the input port twice.

(Example)

```

      :
      :
BP1   AAA      ; 1st polling
BP1   AAA      ; 2nd polling
HALT   ; Standby
      :
AAA:

```

## 2-2. Sample application 2 where the standby function is used for power failure backup

Shown below is a sample application where the program selects between power-ON reset and reset after power is restored.

### 2-2-1. Sample application circuit – (2) (No instantaneous break in power source)

Fig. 2-3 shows a sample application where the standby function is used for power failure backup.

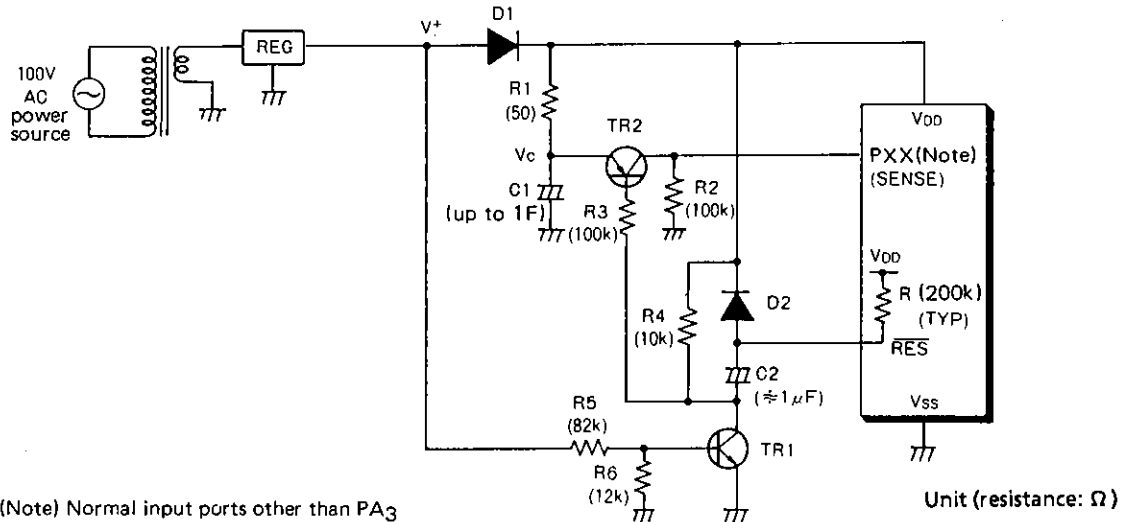
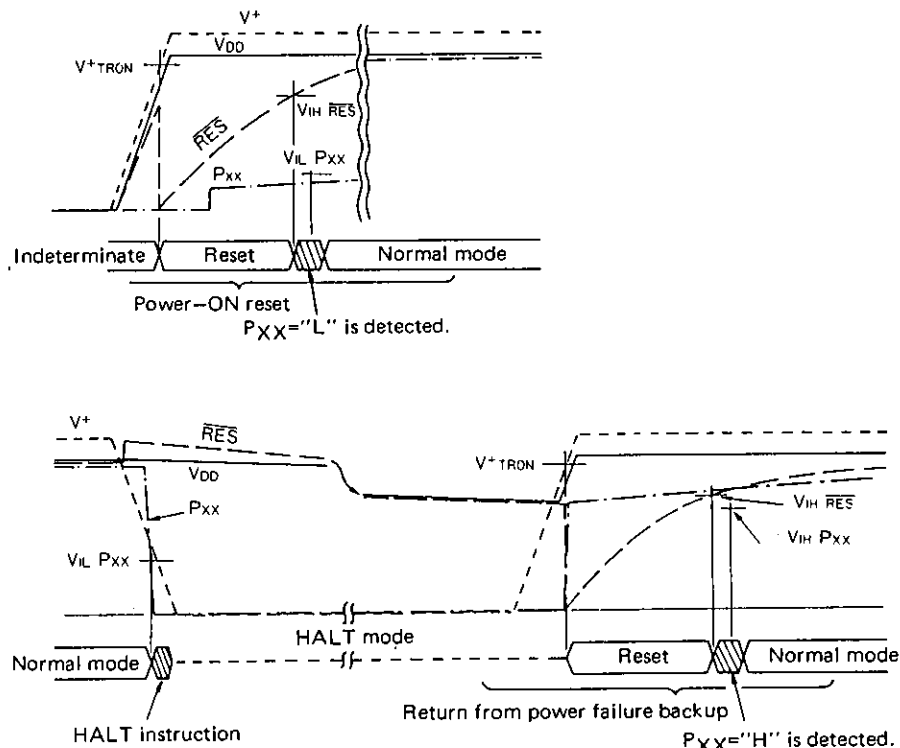


Fig. 2-3 Sample application – (2) where the standby function is used for power failure backup

### 2-2-2. Operating waveform in sample application circuit – (2)

The operating waveform in the sample application circuit in Fig. 2-3 is shown in Fig. 2-4. The mode is roughly divided as follows:

- (1) Power-ON reset
- (2) Return from power failure backup



V<sup>+</sup>TRON: V<sup>+</sup> value when TR1 is turned ON/OFF.

Fig. 2-4 Operating waveform in sample application circuit – (2)

2-2-3. Operation of sample application circuit – (2)

- (a) At the time of power-ON reset  
The operation and notes are the same as for sample application circuit – (1), except that after reset release  $P_{XX}="L"$  is program-detected to decide program start after initial reset.
  - (b) Standby initiation  
When one polling regards the  $P_{XX}$  input voltage as "L" level, the HALT mode is entered.
  - (c) At the time of return from power failure backup  
After power is restored, a reset occurs, releasing the standby mode.  
After standby release  $P_{XX}="H"$  is program-detected, deciding program start after power is restored.
- Note –  
If power is restored after  $V_{DD}$  during power failure backup gets lower than  $V_{IH}$  on the  $P_{XX}$ ,  $P_{XX}="L"$  may be program-detected, deciding program start after initial reset.

2-2-4. Notes for design of sample application circuit – (2)

- R2 and R3  
Fix the R2 value so that  $R2 \gg R1$  is yielded and fix the R3 value so that  $I_B$  of TR2 is limited.
- R4  
There is no severe restriction on the R4 value, but fix it so that C2 can discharge quickly.  
Other notes are the same as for sample application circuit – (1).

2-2-5. Notes for software design

- Design the program so that port A3 is brought to "H" level at the standby mode.
- Check a standby request by polling the input port once.

(Example)

```

      BP1      AAA      ; Polling
      HALT      ; Standby
      |
AAA:
  
```



### 2-3. Sample application 3 where the standby function is used for power failure backup

#### 2-3-1. Sample application circuit – (3) (There is an instantaneous break in power source.)

Fig. 2-5 shows a sample application where the standby function is used for power failure backup.

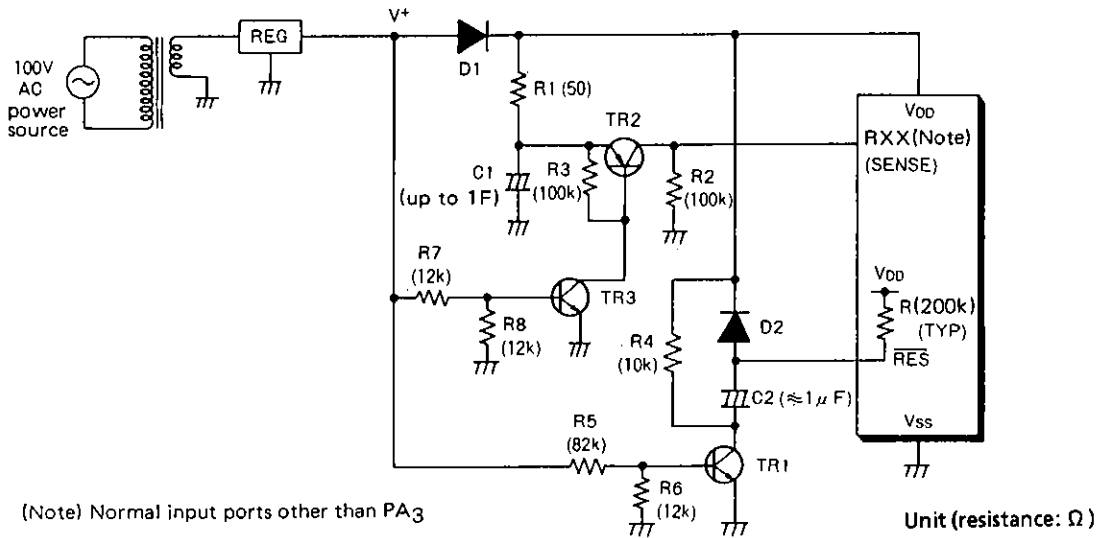


Fig. 2-5 Sample application – (3) where the standby function is used for power failure backup

#### 2-3-2. Operating waveform in sample application circuit – (3)

The operating waveform in the sample application circuit in Fig. 2-5 is shown in Fig. 2-6. The mode is roughly divided as follows:

- (1) Power-ON reset
- (2) Instantaneous break of main power source
- (3) Return from power failure backup

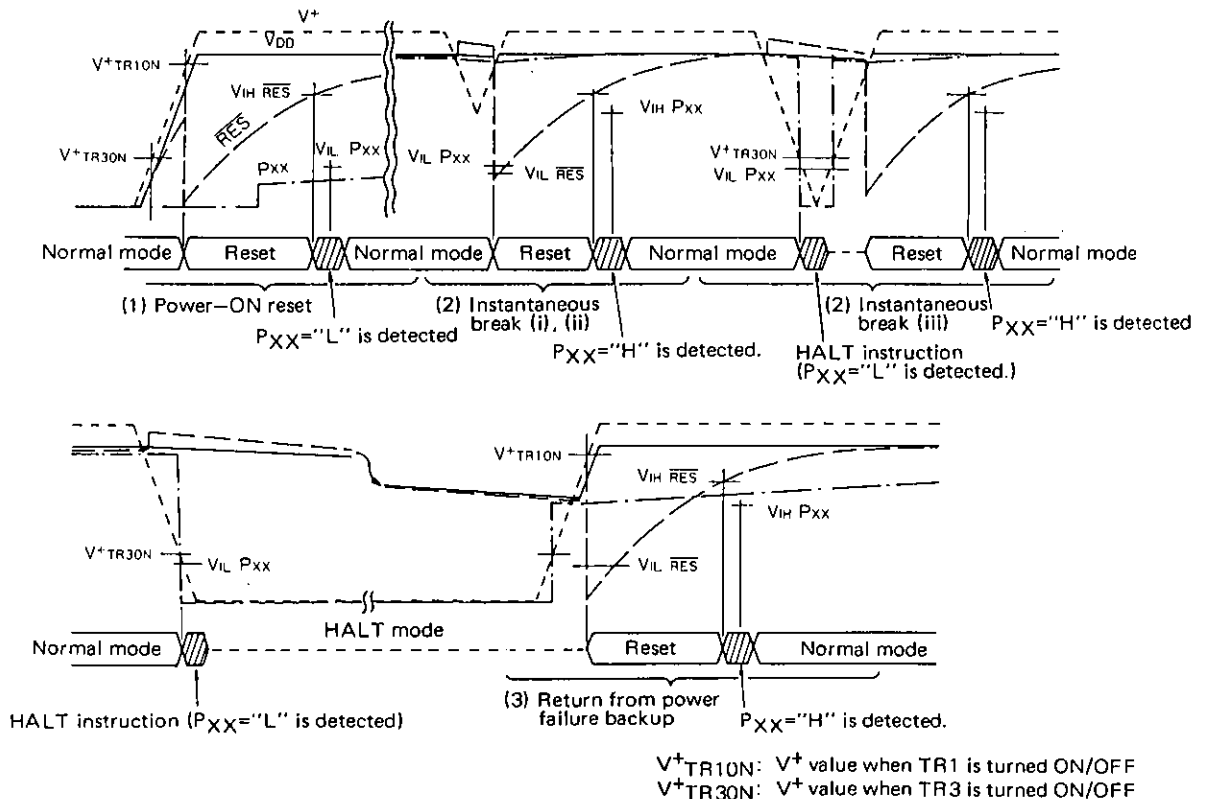


Fig. 2-6 Operating waveform in sample application circuit – (3)

## 2-3-3. Operation of sample application circuit – (3)

## (a) At the time of power-ON reset

The operation and notes are the same as for sample application circuit – (2)

## (b) At the time of instantaneous break

- (i) When the  $P_{XX}$  input voltage does not meet  $V_{IL}$  (the  $P_{XX}$  input level does not get lower than input threshold level  $V_{IL}$ ) and the  $\overline{RES}$  input voltage only meets  $V_{IL}$ :

A reset occurs in the normal mode. After reset release  $P_{XX}="H"$  is program-detected, deciding program start after instantaneous break.

- (ii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage do not meet  $V_{IL}$ :

The program continues running in the normal mode.

- (iii) When both of the  $P_{XX}$  input voltage and  $\overline{RES}$  input voltage meet  $V_{IL}$ :

When two pollings do not regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is not entered and a reset occurs.

When two pollings regard the  $P_{XX}$  input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode. After standby release  $P_{XX}="H"$  is program-detected, deciding program start after instantaneous break.

## (c) At the time of return from power failure backup

The operation and notes are the same as for sample application circuit – (2)

## 2-3-4. Notes for design of sample application circuit – (3)

- R3

Bias resistance of TR2

- R7 and R8

Fix the R7 and R8 values so that TR3 is turned ON/OFF at approximately 1.5V of  $V^+$ .

Other notes are the same as for sample application circuit – (1)

## 2-3-5. Notes for software design

Same as for sample application circuit – (1)

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

- ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.